Q[0:0]

Q1[0:0]

retard_T4

RAM-based Shift Register

A[9:0]   D[0:0]   CLK

Q[0:0]

retard_T5

RAM-based Shift Register

A[9:0]   D[0:0]   CLK

Q[0:0]

AND_2

Utility Vector Logic

Op1[0:0]   Op2[0:0]

Res[0:0]

NOT_2

Utility Vector Logic

Op1[0:0]

Res[0:0]

A[9:0]

D[0:0]

A1[9:0]

CLK

BLOCK 2
F.BLANC
BiGaNver
LAAS-CNRS
2023-10-31