# REX Red Pitaya ADC-DAC démo & Echo Ethernet

Red Pitaya 125-14 STEMlabBoard

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Présentation de la Red STEMlab Board :

## Introduction

La RedPitaya est une carte FPGA « bas coût », une carte de développement comme Arduino ou Raspberry Pi. La particularité de cette carte est sa capacité de gérer des signaux rapides jusqu'à 50MHz. La carte peut être utilisée rapidement avec les applications disponibles, ou peut être exploitée comme une plate-forme ouverte. Il est possible de l'adapter à un grand nombre de projets nécessitant un contrôle rapide et performant comme du traitement de signal ou de la radio logicielle.

C'est une plate-forme d'acquisition et de génération de signaux RF de la taille d'une carte de crédit. La carte est basée sur un système sur puce SOC — FPGA de la gamme Xilinx Zynq qui permet de combiner la capacité de programmation d'un cœur ARM Cortex-A9 à double cœur (LINUX embarqué).

## Schéma de principe et architecture

L'instrument est équipé de deux entrées et deux sorties analogiques RF (125 MS/s). Différentes résolutions sont proposées (10,14 ou 16 bits), quatre entrées et quatre sorties analogiques (100 kS/s), ainsi que de 16 ports entrés/sorties logiques universels. Coté connectivité, nous pouvons compter sur un port ETHERNET 1 Gbit, un port USB 2.0 et autre protocoles (I2C, SPI, UART), le tout peut être autonome grâce à la carte SD.

Pour le soft la carte est basée sur le système d'exploitation GNU/Linux. Possibilité d'intégration dans son propre système/produit, elle peut être programmée avec différents niveaux avec une variété d'interfaces logicielles, les langages de programmation sont : HDL/Verilog, C/C++, Python/Jupyter, et un serveur web intégré (NGINX) pour des interfaces web basées sur HTML/JavaScript. Elle peut être utilisé comme oscilloscope et générateur de signaux, spectre, analyseur de Bode, analyseur logique, compteur LCR\*, streaming, SDR ou analyseur de réseau vectoriel\* grâce à l'écosystème fourni par STEMlab.

On peut également utiliser **PyRPL** (Python Red Pitaya Lockbox), un progiciel open source en Python pour les expériences d'optique quantique contrôlées par FPGA avec des applications disponibles : Lock-in Amplifiers, PID...

## STEMlab Board 125-14 :



Liens utiles sur le site Red Pitaya STEMlab :

https://redpitaya.com/stemlab-125-14/

https://redpitaya.com/rtd-

iframe/?iframe=https://redpitaya.readthedocs.io/en/latest/developerGuide/har dware.html

https://redpitaya.com/applications-measurement-tool/fpga/

https://redpitaya.readthedocs.io/en/latest/developerGuide/software/build/fpga /fpga.html

-> Quick Start

-> Developers guide -> Hardware -> Software STEMlab Board 125-10 versus STEMlab Board 125-14:

		STEMIab 125-10	STEMIab 125-14	
-	Processor	Dual Core ARM Cortex A9	Dual Core ARM Cortex A9	
	FPGA	Xilinx Zynq 7010 SOC	Xilinx Zynq 7010 SOC	
	RAM	256 MB (2 Gb)	512 MB (4 Gb)	
o	System memory	Micro SD up to 32 GB	Micro SD up to 32 GB	
Bas	Console connection	USB to serial converter required	micro USB	
	Power connector	Micro USB	Micro USB	
	Power connector	Micro USB	Micro USB	
	Power consumption	5 V, 1,5 A max	5 V, 2 A max	
A	Ethernet	1 Gbit	1 Gbit	
tivit	USB	USB 2.0	USB 2.0	
Dec	WiFi	requires WIFI dongle	requires WIFI dongle	
S	Synchronisation		Daisy chain connector (up to 500 Mbps)	
	RF input channels	2	2	
	Sample rate	125 MS/s	125 MS/s	
	ADC resolution	10 bit	14 bit	
put	Input impedance	1 MOhm / 10 pF	1 MOhm / 10 pF	ADC :
Li Li	Full scale voltage range	+-20 V	+-20 V	LTC2145-14
œ	Absolute max. Input voltage range	30 V	30 V	
	Input ESD protection	Yes	Yes	
	Overload protection	Protection diodes	Protection diodes	
	RF output channels	2	2	
	Sample rate	125 MS/s	125 MS/s	
22	DAC resolution	10 bit	14 bit	
tpu	Load impedance	50 Ohm	50 Ohm	DAC 🛑
Fou	Voltage range	+-1 V	+-1 V	LTC2145-14
2	Ouput slew rate	200 V/us	200 V/us	
	Short circut protection	Yes	Yes	
	Connector type	SMA	SMA	
	Digital IOs	16	16	
tor	Analog inputs	4	4	
Dec	Analog inputs voltage range	0-3,5 V	0-3,5 V	
con	Sample rate	100 kS/s	100 kS/s	
ion	Resolution	12 bit	12 bit	
Sue	Analog outputs	4	4	
Ext	Analog outputs voltage range	0-1,8 V	0-1,8 V	
, j	Communication interfaces	PC, SPI, UART	I <sup>2</sup> C, SPI, UART	
	Dimensions	107 x 60 x 21 mm	107 x 60 x 21 mm	



#### STEMlab Board : Accès mode local ou adresse IP

Ecosystème installé sur la carte SD :

## Accès local RP-F\*\*\*\*LOCAL/



## Accès distant adresse IP



## Oscilloscope :



## 1. Objectif du TP :

Prendre en main et programmer la RedPitaya avec Vivado « bare metal »,

## C'est à dire sans la carte SD insérée.

La Red Pitaya dispose de 2 interfaces de programmation :

 Une prise micro USB avec une puce FTDI derrière (nommée CON) à l'arrière de la carte.
 Une interface JTAG (pin header nommé JTAG) sur la face avant.

Nous allons utiliser un **câble USB-JTAG Xilinx HS2** pour :

- 1) Programmer sous Vivado 2022 2 le HARDWARE- > ADC-DAC et IP maison
- 2) Programmer le SOFTWARE avec Vitis 2022 2-> Exemple Echo Ethernet.
- 3) Créer un fichier BOOT.bin sur carte SD pour la sauvegarde du programme.
- 4) Utiliser une carte fille développée pour la RedPitaya qui permet une entrée d'horloge externe pour la synchronisation.

Carte fille sur RedPitaya 125\_14 with external Clock



3. Demo RedPitaya sous Vivado 2022\_2

3.1 Bloc design du TP Demo RedPitaya sous Vivado 2022\_2



Vue d'ensemble Demo RedPitaya sous Vivado 2022\_2

## 3.2 Environnement de développement Xilinx (VIVADO)

3.3 Création du projet sous Vivado\_2022\_2 :

Lancer Vivado 2022.2-> File->Project->New->Create new Vivado project-> Next.

Vivado 2022.2 Elle Flow <u>T</u> ools <u>W</u> indow <u>H</u> elp <u>Q</u> . Quick Access			- 0 ×
VIVADO.			<b>E</b> XILINX
Quick Start	New Project	Create a New Vivado Project This wizard will guide you through the creation of a new project.	
Open Project > Open Example Project >		To create a Vixalo projectyto will need to provide a name and a location for your project tiles. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.	
Tasks Manage IP > Open Hardware Manager >			
Learning Center			
Documentation and Tutorials > Quick Take Videos > What's New in 2022.2 >			
	E XILINX.		
	•	< Back Einish Cancel	
Tcl Console			

Create new Vivado project-> project name-> Next.

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Quick Start	Inter Project     Xee Project Name Enter a name for your project and specify a driedowy where the project data files will be stored.	
	Projectname: Red_Pitaya_125_14_demo_ANF_2023	
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Manage IP > Dpen Hardware Manager > /ivado Store >		
Learning Center Documentation and Tutorials > Quick Take Videos > What's New in 2022.2 >		
	Image: Second	

Ici je nomme le projet Red\_Pitaya\_125\_14\_demo\_ANF\_2023

Dans le répertoire Xilinx je créer un dossier-> TP\_VIVADO\_2022\_2

		<b>£</b> XILINX
Quick Start create Project > Open Project > Open Example Project >	Know Project Type      Specify the type of project to create.      (in ERL Project     Tow Wite add is add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.     [D point specify sources at this time	
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Learning Center Documentation and Tutorials > Quick Take Videos > What's New In 2022.2 >	Egympia Projed     Create a new Visido project trum a predefined template.	
	Cancel	

## Sélectionner « RTL Project » pour « Projet Type » puis « Next »

ate a new project

Dans Add Sources et Add Constraint-> On ne spécifie rien-> sélectionner-> Next



La board Redpitaya n'est pas présente par défaut dans Vivado :

Allez sur le lien ci-dessous pour récupérer redpitaya-125-14/1.0

https://github.com/fabzz60/demo\_adc\_dac\_Redpitaya\_125\_14

Copier /coller le dossier board\_files/redpitaya-125-14/1.0 dont on a besoin dans C:\Xilinx\Vivado\2022.2\data\boards redémarrer Vivado.



Dans la fenêtre « **Default Part** », sélectionner « **Boards** », puis redpitaya-125-14 dans l'onglet « Display Name ». Appuyer sur « Next »

Elle Flow Iools Window Help Q-OuldkAccess		
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Open Example Project >	To faith the latest available boards from oil repositiony click on Refresh' button. Discrises	
	Reset All Filters	
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Manage IP		
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Vivado Store >	Display Name         Device         Data/s         Vindor         File Version         Pait           ZoedSourd Zing Education and Devicionment Nat         Xim         Installed         emainstcom         1.4         xt7b202dg464.1	
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what's new in 2022.2 3	Refresh	
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#### Dans la fenêtre « New Project Summary », cliquez sur « Finish » :



L'environnement de Vivado est lancé.

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Nous allons récupérer la bibliothèque IP Redpitaya-125-14

https://github.com/fabzz60/demo\_adc\_dac\_Redpitaya\_125\_14

Copier-coller le dossier <u>IPs adc dac redpitaya 125 14</u> dans le répertoire source de votre projet, pour moi c'est :

C:\Xilinx\TP\_VIVADO\_2022\_2\Red\_Pitaya\_125\_14\_demo\_ANF\_2023

Dans l'onglet PROJECT MANAGER-> Settings -> IP Repository-> clic sur +-> ajouter le dossier : IPs\_adc\_dac\_redpitaya\_125\_14



**Dans l'onglet IP Repository-> Select->** IP\_adc\_dac\_redpitaya\_125\_14-> **Select.** 



Dossier IPs\_adc\_dac\_redpitaya\_125\_14 ajouté

Dans Settings-> sélectionner Apply puis « OK »



## Création du block design :

Dans la fenêtre **"Flow Navigator** » de Vivado à gauche de l'écran, cliquez sur « Create Block Design » de la rubrique « IP Integrator », remplacer le nom donné par défaut au block design par Red\_Pitaya\_demo

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## Puis « **OK** »

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Create and add an IP subsystem in the m	< mind								;	

On va insérer les IP Processeur Zynq et Processeur Reset, ainsi que les IPs\_adc\_dac\_redpitaya\_125\_14 sur le **Diagram** :

- Le Processeur Zynq (Système de traitement ZYNQ7)
- Le Processeur Reset (Réinitialisation du système du processeur)

- AXIGPIO (L'AXI GPIO fournit une interface d'entrée/sortie à usage général) l'interface AXI)
- Redpitaya-125-14-clk
- **Redpitaya-125-14-adc** (les échantillons ADC 14 bits sont alignés MSB dans les interfaces de flux AXI 16 bits sortantes)
- Redpitaya-125-14-dac (les échantillons DAC 14 bits sont extraits du MSB des interfaces de flux AXI 16 bits entrantes)

Red, Pitaya, 125, 14, demo, ANF, 2023, vi	2 - [Cr/Xilini/TP_VIVADO_2022_2/Red_Pitaye_125_14_demo_ANF_2023_v2/Red_Pita	vys.,125.,14.,demin.,ANF_2023_vZ.xpr] - Vivadio 2022.2.	- D ×						
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49 Generate Bitstream	INFO: [IP_Flow 15-234] Refreshing IP repositories								
> Open Hardware Manager	[] INFO: [IP_TAV 14-1700] Loaded user IP repeatory 'cr/Rilino/TP_VINDO_2022_278d_Jitaya_125_14_demo_ANF_2023/IPa_ddc_dac_redpitaya_125_14',								
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#### Dans Diagram -> clic sur + tapez dans la barre de recherche -> Zynq

#### Touche entrée -> le processeur apparait sur le Diagram





#### 🝌 Red Pits Ready I Default Layout ~ ? × PROJECT MANAGER Sources Design x Signals Board ? \_ 🗆 🖄 Diagram x Address Editor x Address Map x ? 🗆 🖸 Settings 이 폰 네 ٥ ٥ Add Sources Connections processing\_system7\_0 (2YN07 P) Language Templates IP Catalog V IP INTEGRATOR Create Block Design Open Block Design processing\_system7\_0 Generate Block Design DDR FIXED\_IO ✓ SIMULATION Run Simulation Block Properties ? \_ C 🛙 X processing\_system7\_0 ← → 0 Y RTLANALYSIS > Open Elaborated Design Name: processing\_system7\_0 (2) Parent name: Red\_Pitaya\_demo ZYNQ7 Processing System ✓ SYNTHESIS Run Synthesis > Open Synthesized D General Properties IP IMPLEMENTATION Run Implementation Tcl Console × Messages Log Reports Design Runs ? \_ 0 6 > Open Implemented Design Q. <u>∓</u> ≑ || ⊡ ⊞ ш create\_bd\_cell -type ip -vinv miling.com/pprocessing\_system?(5.5 processing\_system?\_0 create\_bd\_cell: Time (s): cpu = 00:00:03 ; elapsed = 00:00:08 . Memory (MB): peak = 1921.375 ; gain = 38.035 sectorum Y PROGRAM AND DEBUG 👫 Generate Bitstream endprop deter, pi, dys. (r.d., colls processing\_system?.) deters (r.d.)sy, (r.d., colls processing\_system?.) statigroup restrictions restrictions restrictions restrictions response respon > Open Hardware Manage I Type a Tol command here

#### Clic sur Run Block Automation-> puis « OK »

Dans **Diagram** -> clic sur + tapez dans la barre de recherche -> **processor system** reset



#### Touche entrée -> le processeur system reset apparait sur le Diagram



Dans Run Connection Automation-> sélectionnez ext\_reset\_in et new Clocking Wizard-> puis « OK »

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> Open Hardware M				
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Block Pin: slowest sync cl	ik			





Dans **Diagram** -> clic sur + tapez dans la barre de recherche -> **AXI GPIO** 

Dans PROJECT MANAGER-> IP Catalog-> sélectionnez User\_Repository-> Add IP to Block Design / On ajoute les trois IP sur le Block Design



Les IP ADC DAC et CLK apparaissent



Nous utilisons *clk\_125*, qui fonctionne à 125 MHz, pour piloter la logique principale de la conception. Tous les chemins de données de ce didacticiel seront synchrones avec cette horloge. Connectez les horloges et les réinitialisations comme indiqué dans le Diagram ci-dessous.



Configurez l'AXI GPIO pour avoir une sortie 4 bits qui correspond aux Leds de la RedPitaya que l'on va utiliser pour tester l'Echo Ethernet

## **Double clic** sur AXI\_gpio\_0

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	INFO: [Common 17-17] undo '	1	OK Cancel	n <sup>-</sup>
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#### Sélectionnez GPIO et GPIO Width = 4 puis « OK »

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	to article and the set of the se	,Ū

#### Clic sur Run Connection Automation-> puis « OK »

Il nous reste à câbler manuellement comme ci-dessous les lignes d'horloges.



Nous allons importer les IP « maison » du projet : récupérer divide\_clock.vhd

Frequency\_modulation.vhd, leds.vhd, Select\_in\_data.vhd avec le lien cidessous : https://github.com/fabzz60/demo\_adc\_dac\_Redpitaya\_125\_14

→ → ↑ 👛 → Ce PC → OS (Ci) → Xilinx → TP_VIVADO_20	022_2 > Red_Pitaya_125_14_demo_ANF_2023			~	C	Rechercher dans : Red_Pitaya_125_14_demo_ANF_2023	
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Copier-coller dans le répertoire du projet.

Nous allons les intégrer à notre projet dans le Diagram RedPitaya\_demo

## Dans BLOCK DESIGN-> clic sur + -> Add or create sources.

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#### On sélectionne les fichiers VHDL puis « OK »



#### Puis « Finish »

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Specify and/or create source files to add to t	he project		



Clic droit sur chaque fichier VHDL puis-> Add Module to Block Design

Les modules insérés sur le Diagram du projet



Nous allons ajouter une IP Xilinx DDS dans le projet : DDS Compiler puis-> touche entrée



### IP ajouté



Double clic sur l'IP DDS Compiler : on configurer l'IP pour générer une modulation de fréquence de 125KHz-> dans **configuration**-> sélectionnez comme ci-dessous

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## Dans implementation-> sélectionnez comme ci-dessous

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## Dans Output Frequencies-> sélectionnez comme ci-dessous

## Dans Summary-> On vérifie que l'on génère un signal @125KHz sur 16bits

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osi elas provi pesign	Optimization Goal	Area (Auto)	FOLK_OLK0
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Pour finir il nous faut câbler manuellement les modules VHDL **insérés comme cidessous** : nous allons utiliser les ADC et DAC de la RedPitaya avec les IP « maison » développées en VHDL.

## Rôle des IP « maison » :

Le module **select\_in\_data** : permet de sélectionner les signaux d'entrées des deux DAC. Deux BP sur la carte fille permettent la sélection des data-> Les signaux sont issus des ADC1 et ADC2 ou des IP internes **Frequency\_modulation** et **DDS\_Compiler**.

Le module **divide\_clock** : permet de diviser l'horloge@125MHz vers 1Hz et visualisé sur des Leds de la carte fille.

Le module Leds : Gérer les Leds de la RedPitaya.

Relier les modules comme ci-dessous :



Enfin il faut câbler les ports d'entrées-sorties :

Par exemple on se place sur l'entrée adc\_clk\_n\_i : clic droit puis

**Create Port** (Ctrl + K) ou **Make External** (ctrl + T).

Attention seul Create Port vous permet de renommer la broche.

#### Faire de même pour toutes les autres entrées-sorties.

### Zoom sur le **Diagram**



#### Vue complète Vivado :



Pour finir mous allons modifier la sortie de axi\_gpio\_0 comme ci-dessous :



Renommer la sortie : leds\_GPIO\_zynq



#### Le module AXI GPIO et sa sortie sur 4 bits



On agence automatiquement le Design



#### On valide le Diagram



Création du HDL Wrapper :
Dans l'onglet **Sources /Hierarchy** du BLOCK DESIGN « Red\_Pitaya\_demo », clic droit et sélectionnez « **Generate Outputs Products** », « **Generate** » puis « **OK** »



# Generate Outputs Products ...



Dans l'onglet « Red\_Pitaya\_demo », clic droit et sélectionnez « Create HDL Wrapper » :



#### Let vivado manage wrapper... puis-> OK.



#### Wrapper crée !



#### Arborescence complète !



### Ajout ou création d'un fichier de contrainte :

Dans PROJECT MANAGER-> Sélectionnez dans Add Sources-> « Add or create constraints »-> Next>



Nous allons récupérer le fichier de contrainte dans le dossier source du projet : CmodA7.xdc : Sélectionnez redpitaya.xdc puis « **OK** »

https://github.com/fabzz60/demo\_adc\_dac\_Redpitaya\_125\_14

Add or Create Constraints-> Add Files-> Next.

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# Sélectionnez redpitaya.xdc puis « OK »



#### Finish...



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#### On lance la synthèse-> touche F11

#### Save...



#### Clic sur « OK »

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### On ouvre l'implémentation :



#### Implémentation...

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# Vérification par rapport au fichier de contrainte redpitaya.xdc

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On fait une sauvegarde pour une mise à jour du fichier de contrainte : CmodA7.xdc-> **CTRL + S** 

# Dans Flow Navigator-> Run Implementation

Pho       Disk	Red_Pitaya_125_14_demo_ANF_2023_v2	- [C:/Xilinx/TP_VIVADO_2022_2/R	ed_Pitaya_125_14	_demo_ANF_2023_v2/Red_Pitaya_	125_14_dem	o_ANF_2023	[_v2.xpr]	- Vivado 2	022.2											-	ð X
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Rud Smulaton <ul> <li>Presence_1254/Elihandra(Hergence_notabatench())</li> <li>StateL_modelinearia(Hergence_notabatench())</li> <li>Sta</li></ul>	V SIMULATION	> • Red_Pita	ya_demo(STRU)	CTURE) (Red_Pitaya_demo.shid)	(13)	98	set_	property	PACKAGE_	PIN F16 [ge	ports (leds	GPIO_zyng[0]	11								
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Générer le bit file pour programmer la cible FPGA partie HARDWARE



Launch Runs-> « **OK** »

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#### Bitstream OK



Dans Flow Navigator-> Open Hardware Manager-> Open Target-> Auto connect.



#### A ce stade on ne programme que le HARDWARE via le câble JTAG-USB.

### Open Target-> Auto connect.



Hardware Manager -> Program Device->Program



Dans l'onglet Program Device vérifier le nom et le chemin du projet...

#### On ferme HARDWARE MANAGER-> clic sur « OK »

<ol> <li>Red_Pitaya_125_14_demo_ANF_2023_v</li> </ol>	2 - [C:/Xilina/TP_VIVADO_2022_2/Red_Pitaya_125_14_demo_ANF_2023	y2/Red_Pitaya_125_14_demo_ANF_2023_y2.apri} - Vivado 2022.2	- 0 ×
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Y PROGRAM AND DEBUG			
Generate Bitstream	· · ·		, ×
✓ Open Hardware Manager	Type a Tol command here		
	AL .		

Important : Avec la programmation du bit file sur vivado :

On peut vérifier sur la carte RedPitaya le fonctionnement des ADC-DAC avec les fréquences générées par l'IP DDS Compiler et l'IP maison frequency\_modulation

en utilisant les boutons poussoirs. On visualise également l'état des leds (leds\_redpitaya [3 :0]) cadencés@1Hz sur la carte fille, et les leds sur la carte RedPitaya (leds\_GPIO\_zynq [3 :0]) cadencés également @1Hz.

Fonctionnement de la carte Redpitaya 125\_14 après chargement du programme



Fréquences générées par l'IP DDS et l'IP maison @125KHz



Exporter vers VITIS le projet VIVADO 2022.2

Menu principal-> File-> Export-> Export Hardware

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#### Next...



Export Hardware-> Include bitstream-> Next.



#### Next...



#### Finish

![](_page_52_Picture_0.jpeg)

# On lance VITIS 2022\_2

Menu Tools-> Launch Vitis IDE

![](_page_52_Picture_2.jpeg)

Ele Edit Flow Tools Reports Window Layout View Help write\_bitstream Complete 🖌 E, + + E . III Default Layout Create and Package New IP... Create Interface Definition. \_14\_demo\_ANF\_2023\_v2 Enable Dynamic Function eXchange V IP INTEGRATOR Enable Dynamic Function eXchange... <u>B</u>un Tid Script... Property Editor Associate EL<u>F</u> Files... Generate Memory Configuration File... Compile Simulation Libraries... ? \_ □ □ × redpitaya.xdc ? 🗆 🗆 X Create Block De ۰ C:/Xilimx/TP\_VWADO\_2022\_2/Red\_Pitaya\_125\_14\_demo\_ANF\_2023/redpitaya.xdc Open Block Desig ¢ Generate Block D STRUCTURE) (Red Pitava demo wr. per(STRUCTURE) (Red\_Pilaya\_demo\_wrappe (Red\_Pilaya\_demo (Red\_Pilaya\_demo.bd) (1) STRUCTURE) (Red\_Pilaya\_demo.bd) (13) sraf) (Frequency\_modulation.ind) Pointer to Jate Vidd) ✓ SIMULATION Vivado Store Run Simulation Cystom Comman Select\_in\_data Open Elaborated
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Lauch Vitis...

![](_page_53_Figure_0.jpeg)

#### Environnement Vitis

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# Projets déjà existants...

Dans Menu Principal->File->New-> Platform Project

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Rename the project-> redpitaya\_ANF-> Next.

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Dans Create a new platform hardware (XSA)-> Browse...

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New Application Project-> LwIP Echo Server

La librairie n'est pas active par défaut dans le projet : on doit revenir dans le BSP

Pour activer IwIP Echo Server : donc faire Cancel

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![](_page_60_Figure_1.jpeg)

# On retrouve installé la librairie lwip211\_v1\_8

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On reprend la précédente procédure : Menu principal->File-> New-> Application Project

![](_page_62_Figure_2.jpeg)

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Le projet complet : En vert la platform HARDWARE en rouge la partie SOFTWARE Zynq avec l'exemple Echo Ethernet

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On va modifier les fichiers sources du programme : main.c et echo.c et insérer deux nouveaux fichiers : leds\_RGB.c Led\_RGB.h au projet pour la gestion et la communication avec les leds de la RedPitaya en Ethernet.

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Fermer VITIS 2022\_2!

Télécharger les fichiers main.c, leds\_RGB.c, leds.RGB.h, echo.c avec le lien <u>https://github.com/fabzz60/demo\_adc\_dac\_Redpitaya\_125\_14</u>

Copier- coller dans le répertoire du projet Vitis les fichiers ci-dessus :

Le chemin d'accès devrait ressembler à ceci :

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> R leds RGB.h	140 WEINAS	++ print_app_header(): void
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3 23 lige	150 garage alde = 0;	print_ip_settings(ip_addr_t*, ip_addr_t*, ip_addr_t*) : void
😾 redpitaya_ANF2023.prj	158 Palse	
o 🍋 Lide	159 /* initialize IP addresses to be used */	ProgramSfpPhy(void) : int
V 🕞 Debug	160 IP4_ADDR(&ipaddr, 169, 254, 17, 45);	ji⊂PhyReset(void) : int
) Cas sd card	161 IP4_ADDR(&netmask, 255, 255, 255, 0);	e main() : int
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/redpitaya_ANF2023/src/main.c		

C:\Xilinx\TP\_VIVADO\_2022\_2\Projets\_VITIS\_2022\redpitaya\_ANF2023\src

Sauvegarder: **Ctrl +SHIFT + S** puis clic droit sur redpitaya\_ANF2023\_system-> **Build Project** 

Dans le main.c On vérifie l'adresse IP et l'adresse MAC de la redpitaya

67

Projets_VITIS_2022 - redpitaya_ANF2023/src/main.c - Vitis IDE     Edia Sarah Run View Branch Mindam Idata		- 0 ×
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Pour retrouver l'adresse IP et MAC de la Redpitaya il faut la carte SD insérer et le système d'exploitation Red Pitaya préchargé</mark> :

https://redpitaya.readthedocs.io/en/latest/quickStart/SDcard/SDcard.html

![](_page_67_Picture_3.jpeg)

Procédure pour une connexion Ethernet directe :

Windows (le service Bonjour doit être installé pour Win 7/8)

1. Connectez le câble Ethernet et attendez env. 30 secondes

2. Ouvrez le navigateur Web et tapez **rp-xxxxxx.local/** dans le champ URL

# Linux/Ubuntu

- Ouvrez les paramètres réseau, modifiez la connexion et, pour le réseau LAN, sélectionnez Méthode Partager avec d'autres ordinateurs sous Paramètres IPv4.
- 2. Connectez le câble Ethernet et attendez env. 30 secondes
- 3. Ouvrez le navigateur Web et tapez **rp-xxxxx.local/** dans le champ URL

![](_page_68_Picture_7.jpeg)

Adresse IP dans System

Une dernière chose est nécessaire pour la communication Ethernet avec la redpitaya et notre programmation Bare Metal, c'est de modifier le fichier xemacpsif\_physpeed.c dans le BSP de la platform project Redpitaya\_ANF.

Chemin d'accès du fichier xemacpsif\_physpeed.c :

C:\Xilinx\TP\_VIVADO\_2022\_2\Projets\_VITIS\_2022\redpitaya\_ANF\ps7\_cortexa9 \_0\standalone\_domain\bsp\ps7\_cortexa9\_0\libsrc\lwip211\_v1\_8\src\contrib\p orts\xilinx\netif\ **xemacpsif\_physpeed.c** 

Le contrôleur HARDWARE PHY LANTIQ sur la Redpitaya n'est pas inclus dans la librairie **lwip211\_v1\_8....** Gasp ! :(

Ouvrir le fichier xemacpsif\_physpeed.c dans Vitis comme ci-dessous :

![](_page_69_Figure_4.jpeg)

Récupérer le fichier xemacpsif\_physpeed.c sur https://github.com/fabzz60/demo\_adc\_dac\_Redpitaya\_125\_14

Effacer l'ancien contenu et copier- coller entièrement le nouveau dans le fichier ouvert sur VITIS ci-dessus.

Sauvegarder: Ctrl +SHIFT + S puis clic droit sur redpitaya\_ANF-> Build Project

![](_page_70_Picture_0.jpeg)

Dans menu Explorer de Vitis-> Clic droit sur redpitaya\_ANF2023 [standalone on ps7\_cortexa9\_0]

Run As-> Launch Hardware ( single application debug)

![](_page_70_Picture_3.jpeg)

Launch Hardware...

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On va sauvegarder le projet complet sur une carte SD en faisant une image du projet : Dans le menu principal-> Xilinx-> Create Boot Image-> Zynq

![](_page_71_Picture_2.jpeg)
C:/Xilinx/TP\_VIVADO\_2022\_2/Projets\_VITIS\_2022/redpitaya\_ANF2023\_system/\_ ide/bootimage/redpitaya\_ANF2023\_system.bif



### Dans Create Boot Image-> Create Image

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echo_cora_z7_system	a all rights reserved.	Leds_RGB.h
moteur_pas_a_pas	4 *	1 xparameters.h
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📑 redpitaya_ANF	6 * are persitted provided that the following conditions are met:	sleep.h
📰 redpitaya_ANF2023_system { redpitaya_ANF }	7 *	netif/xadapter.h
<ul> <li>redpitaya_ANF2023 [ standalone on ps7_cortexa9_0 ]</li> </ul>	8 1. Redistributions of source code must retain the above copyright notice, the block of conditions and the following distributions.	platform.h
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a respiraje_rive_cocsystem.spij	20 * EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT	ten faittenthoid) unid
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reopitaya_system	22 * INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN	++ tcp_slow(mi(void) : void
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stepper_motor_board_OFF_nexys_A7	25 ° OF SUCH DAVIGE.	24 dhcp_start(struct netd")   err_t
stepper_motor_board_OFF_system	27 */	* TopPast ImrPlag : volable int
stepper_motor_nexysA7	28	TcpSlowTmrFlag: volatile int
i stepper_system_system	23 #include <stdio.h></stdio.h>	server_netif : struct netif
test_CORA_board	30 #include "Leds_R68.h"	echo_netif : struct netif*
	31 #include "xpanameters.h"	print_ip6(char*, ip_addr_t*) : void
	32 #include "xil_types.h"	print_ip(char*, ip_addr_t*) : void
	33 #include sleep.m"	print_ip_settings(ip_addr_t*, ip_addr_t*, ip_addr_t*) : void
	34 //include Xapi.n / "Light de peripherique sel -/	→ ProgramSiS324(void): int
		ProgramStpPhy(void) : int
moteur pas a pas (Platform)	37 #include "platform.h"	14 licPhyReset(void) : int
redoitava ANE [Platform]	38 #include "platform_config.h"	main() int
radiationa ANE2023 materia (Sustain)	39 #if defined (arm)    defined(aarch64)	
a contract AME2022 (Application)	40 #include "xil_printf.h"	
Optimized and the second property of the second secon	41 mendif	
2 Palazza	42 43 Sinclude "Jain/tro b"	
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stepper_motor_board_OFF_nexys_A7 (Platform)	Bostoen	PD 354   14
stepper_motor_nexysA7 (Platform)	1	0.11
test_CORA_board [Platform]	****** xilinx Bootgen v2022.2.0	
	**** Build date : Oct 13 2022-12:22:51	V C APU
	** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.	S <sup>O</sup> AKM Cortex-A9 MPCore ≠0 (Kunning)
		ARM Cortex-A9 MPCore #1 (Running)
	WARDING: Partition TsDL.elf.8 range is overlapped with partition Red Pitaya demo wrapper.bit.8 memory range	🥐 xc7z010
	[Newstand]: Partition Res_risys_memo_mrapper.oit.o range 15 overlapped with partition redpitays_Rer2025.elf.0 memo	V Fange St. Debugger_redpitaya_ANF2023-Default (Local)
	[INFO] : Bootimage generated successfully	V 🦉 APU
		ARM Cortex-A9 MPCore #0 (Running)
		ARM Cortex - A9 MPCore #1 (Running)
		20. 2000

Bootimage generated successfully!

Fichier Boot dans: C:\Xilinx\TP\_VIVADO\_2022\_2\Projets\_VITIS\_2022\redpitaya\_ANF2023\_system\\_ ide\bootimage\**BOOT.bin** 

Copier-coller le fichier **BOOT.bin** sur une micro-SD via un adaptateur SD to micro-SD et l'insérer dans l'emplacement micro-SD de la Redpitaya.

Redémarrer la Redpitaya et tester le programme.

Fin de la Démo ADC/DAC avec Echo Ethernet !

# Script Python Echo ethernet



#-\*- coding : utf-8-\*-

import tkinter # import de tkinter

import socket

#### import time

#import sys

HOST = "169.254.17.45" # Standard loopback interface address (localhost)

**PORT = 7** # Port to listen on (non-privileged ports are > 1023)

print('Create a socket on the host PC client.')

lwIP\_socket = socket.socket(socket.AF\_INET, socket.SOCK\_STREAM)

print('Connect to the socket of the lwIP server listening on the redpitaya')

lwIP\_server\_address = (HOST, PORT)

lwIP\_socket.connect(lwIP\_server\_address)

def echo\_packet(lwIP\_socket, message):

message\_byte = message.encode()

lwIP\_socket.sendall(message\_byte)

bytes\_buffer\_size = 32 bytes\_received = 0 bytes\_total = len(message) while bytes\_received < bytes\_total: message\_recvd = lwIP\_socket.recv(bytes\_buffer\_size) bytes\_received += len(message\_recvd) print(message\_recvd)

### try:

#### while True:

message = 'LEDO on' echo\_packet(lwIP\_socket, message) time.sleep(0.5) message = 'LED1 on' echo\_packet(lwIP\_socket, message) time.sleep(0.5) message = 'LED2 on' echo\_packet(lwIP\_socket, message) time.sleep(0.5) message = 'LED3 on' echo\_packet(IwIP\_socket, message) time.sleep(0.5) message = 'LED0 off' echo\_packet(IwIP\_socket, message) time.sleep(0.5) message = 'LED1 off' echo\_packet(lwIP\_socket, message) time.sleep(0.5) message = 'LED2 off' echo\_packet(IwIP\_socket, message) time.sleep(1) message = 'LED3 off' echo\_packet(lwIP\_socket, message)

```
time.sleep(1)
message = 'All LEDs on'
echo_packet(IwIP_socket, message)
time.sleep(1)
message = 'All LEDs off'
echo_packet(IwIP_socket, message)
time.sleep(1)
```

#### finally:

print('Closing the socket from the host PC client side...')

lwIP\_socket.close()

Ouvrir Putty et le port USB-série (COMx) correspondant à la carte Redpitaya détecté et visualiser les infos ci-dessous.





### Test Bench module VHDL frequency\_modulation@125KHz:

## Calcul des points sur Excel :



Calcul des points sous Matlab :

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