*Product Preview*

*TI DN 2509931*

*September 2008*

# DLP® Discovery™ 4000 Starter Kit Technical Reference Manual (Product Preview)

This document describes the functionality of the Texas Instruments DLP® Discovery™ 4000 Starter Kit. The starter kit provides a reference design and development platform for the DDC4000 chipset. The DDC4000 chipset consists of a DDC4000 controller, DAD2000 power and reset drivers, and 2XLVDS DMD.

| Revisions | | |
|---|---|---|
| Rev | Description | Date |
| A | Initial release. | 4/16/08 |
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## IMPORTANT NOTICE

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## Notational Conventions

This document uses the following conventions.
The Discovery™ 4000 Controller Board is also referred to as Controller Board.
Program listings, program examples, and interactive displays are shown as a special typeface similar to a typewriter's. Some examples use a **bold version** of the special typeface for emphasis; interactive displays use a **bold version** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Here is a sample program listing:

```
0011 0005 0001 .field 1, 2
0012 0005 0003 .field 3, 4
0013 0005 0006 .field 6, 3
0014 0006 .even
```

In syntax descriptions, the instruction, command, or directive is in a **bold typeface** font and parameters are in an *italic* typeface. Portions of the syntax that are **bold** should be entered as shown; portions of syntax that are in italics describe the type of information that should be entered. Syntax that is entered on a command line is centered. Syntax that is used in a text file is left justified.
Square brackets (**[**and**]**) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

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This book may contain cautions and warnings.

**This is a description of a caution statement:**

A caution statement describes a situation that could potentially damage your software or equipment.

**This is a description of a warning statement:**

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**Abbreviations and Acronyms**

The following lists abbreviations and acronyms used in this manual.

| | |
|---|---|
| **APPSFPGA** | Xilinx Virtex 5 Field Programmable Gate Array for customer applications |
| **CDS** | Customer Data Sheet |
| **DAD2000** | DMD Power and Reset Driver |
| **D4000** | Discovery™ 4000 |
| **dc** | Direct Current |
| **DDR** | Double Data Rate |
| **DMD** | Digital Micromirror Device |
| **DLP** | Digital Light Processing |
| **DMA** | Direct Memory Access |
| **DRAM** | Dynamic Random Access Memory |
| **DRC** | DAD Reset Controller |
| **DVI** | Digital Video Interface |
| **EMI** | Electromagnetic Interference |
| **FCC** | Federal Communications Commission |
| **FPS** | Frames per Second |
| **FPGA** | Field Programmable Gate Array |
| **HSC** | High-speed Controller |
| **HSP** | High-Speed Port |
| **KnowledgeBase** | Texas Instruments Extranet providing Discovery™ documentation, available after purchase only. |
| **LED** | Light Emitting Diode |
| **PROM** | Programmable Read Only Memory |
| **SCP** | Serial Communications Port |
| **SRAM** | Static Random Access Memory |
| **USB** | Universal Serial Bus |

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# 1 Overview

The DLP® Discovery™ 4000 Starter Kit brings a new level of resolution and performance to the Texas Instruments DLP Discovery™ product group. The Discovery™ 4000 Starter Kit may be used as a development platform to support new uses of DLP™ technology.

The Discovery™ 4000 provides substantial performance improvements including increased data rate, frame rate and resolution. Fast pixel level control of the DMD is provided through the DDC4000 control bus. Both USB and EXP standard compatible I/O connectors provide a flexible platform for advanced DMD product development. The Discovery™ 4000 supports the 2XLVDS DMD devices shown in Table 1:

| TYPE | DMD_TYPE | #COLS | #ROWS | Global Reset Max FPS | Phased Reset Max FPS | #CLKS/ ROW | #DIN |
|---|---|---|---|---|---|---|---|
| .9 1080p Type A | 000 | 1920 | 1080 | 17636 | 23148 | 16 | 64 |
| .7 XGA Type A | 001 | 1024 | 768 | 22614 | 32552 | 16 | 32 |
| .55 XGA Type A | 010 | 1024 | 768 | 22614 | 32552 | 16 | 32 |
| .55 XGA Type X | 011 | 1024 | 768 | 22614 | 32552 | 16 | 32 |

*Table 1 Discovery™ 4000 DMD Types*

The Discovery™ 4000 Starter Kit combines the high performance DLP® Discovery™ 4000 Chip Set with a user programmable Application FPGA (APPSFPGA).

The Virtex 5 Application FPGA provides a user programmable platform for developing custom applications. The Application FPGA is connected to EXP Expansion Connectors providing compatibility with Avnet EXP compatible FPGA development products and connection for custom interfaces. An onboard USB interface provides a convenient interface for rapid prototyping. Connection for DDR2 SO-DIMM memory and SPI Flash Memory to the Application FPGA is included for customer use. A Cypress 68013 USB controller is included for customer USB control applications.

This document is provided to facilitate use of the controller board and to provide a reference design for custom hardware development.

## *1.1 The Discovery™ 4000 Starter Kit*

The Discovery™ 4000 (D4000) Starter Kit provides a development platform for general application of the DMD. The D4000 starter kit includes the following:

- D4000 Controller Board
- DMD board, DMD and flex cable(s)
- Documentation Access through KnowledgeBase™
- Power cable

Not included are:

- Lab power supply, 5V @ 5A
- Xilinx DLC9G programming cable

The D4000 Controller Board provides a complete interface (USB or EXP), data manipulation (via the Virtex 5, SDRAM), DMD Control (via the DDC4000, DAD2000, and DMD) solution for new applications of DLP™ Technology.

Figure 1 is a simplified block diagram of the D4000 Starter Kit.

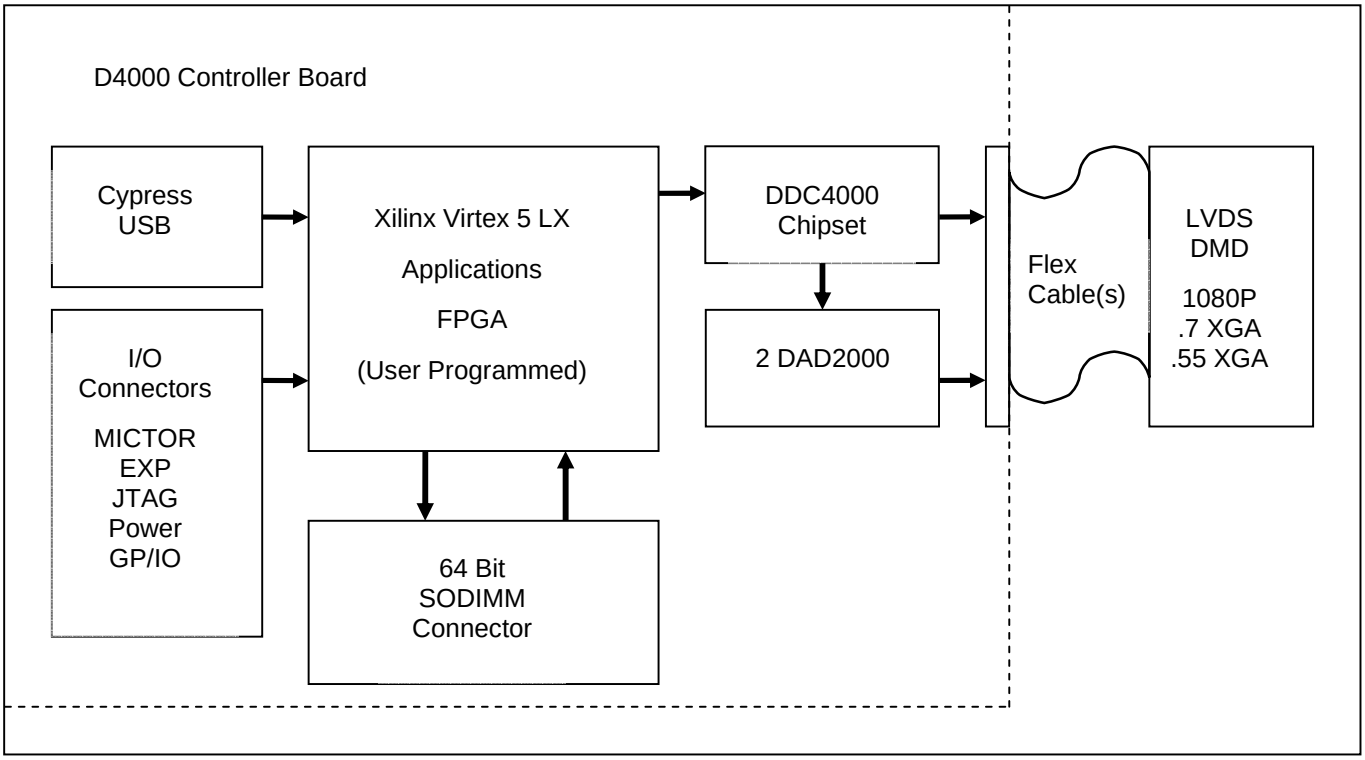


*Figure 1 Discovery™ 4000 Starter Kit Block Diagram*

The controller board contains:

- Two DAD2000 DMD Power and Reset Driver
  - Generates reset control of 16 banks of DMD mirrors
  - Supports higher reset frequencies

    - One DAD2000 required for XGA operation, two for 1080p operation
- DDC4000 Digital Controller
    - Provides high speed 32/64 bit LVDS data and control user interface
    - Provides data and control interface to the DMD and DAD2000
- 32/64 bit 400 MHz DDR DDC4000 Data Interface
    - 32 bit interface for XGA operation, 64 bit interface for 1080p operation
- 5V power input connector
    - On-board regulation of other power supplies included
- A Xilinx Virtex XC5VLX50 Application FPGA (APPSFPGA)
    - For user development of interface and data manipulation functions.
- A 64 bit DDR2 SODIMM Connector
    - For end user development of image storage.
- An Onboard Cypress 68013A USB controller
    - For end user development of USB interface
- EXP Expansion Connectors
    - To connect to an Avnet EXP compatible motherboard product.
    - Board design includes additional LVDS pairs to support 64 bit LVDS connection through EXP connectors with a custom interface board.
- Flash Memory
    - For end user development of no-volatile storage.
- Various I/O connectors
    - Mictor test connectors for logic analyzer connection
    - JTAG headers for device programming
    - GPIO for general purpose digital IO
    - DSP Video In for connection to TI DSP development products.

## *1.2 Development Features*

The Discovery™ 4000 Starter kit provides a development solution for the integration of DLP® Discovery™ 4000 technology into new applications of DLP™. Features include:

- A user programmable Xilinx Virtex 5 XC5VLX50 applications FPGA (APPSFPGA)
- Platform Flash PROM XCF16P to load the APPSFPGA
- JTAG connector for APPSFPGA programming
- Battery support for the APPSFPGA security encryption

- EXP connectors for connection to an EXP compatible board or other accessory board.
- Flash memory for developer use
- Cypress 68013A USB for developer use
- 64 Bit DDR2 SODIMM connector for developer use

### *1.3 Discovery™ 4000 Photo*

The Discovery™ 4000 with 1080p DMD is shown below.

*Figure 2 Discovery™ 4000 Photo*

## *1.4 Key Components*

Figure 3 shows the D4000 Controller Board key components covered in this section.

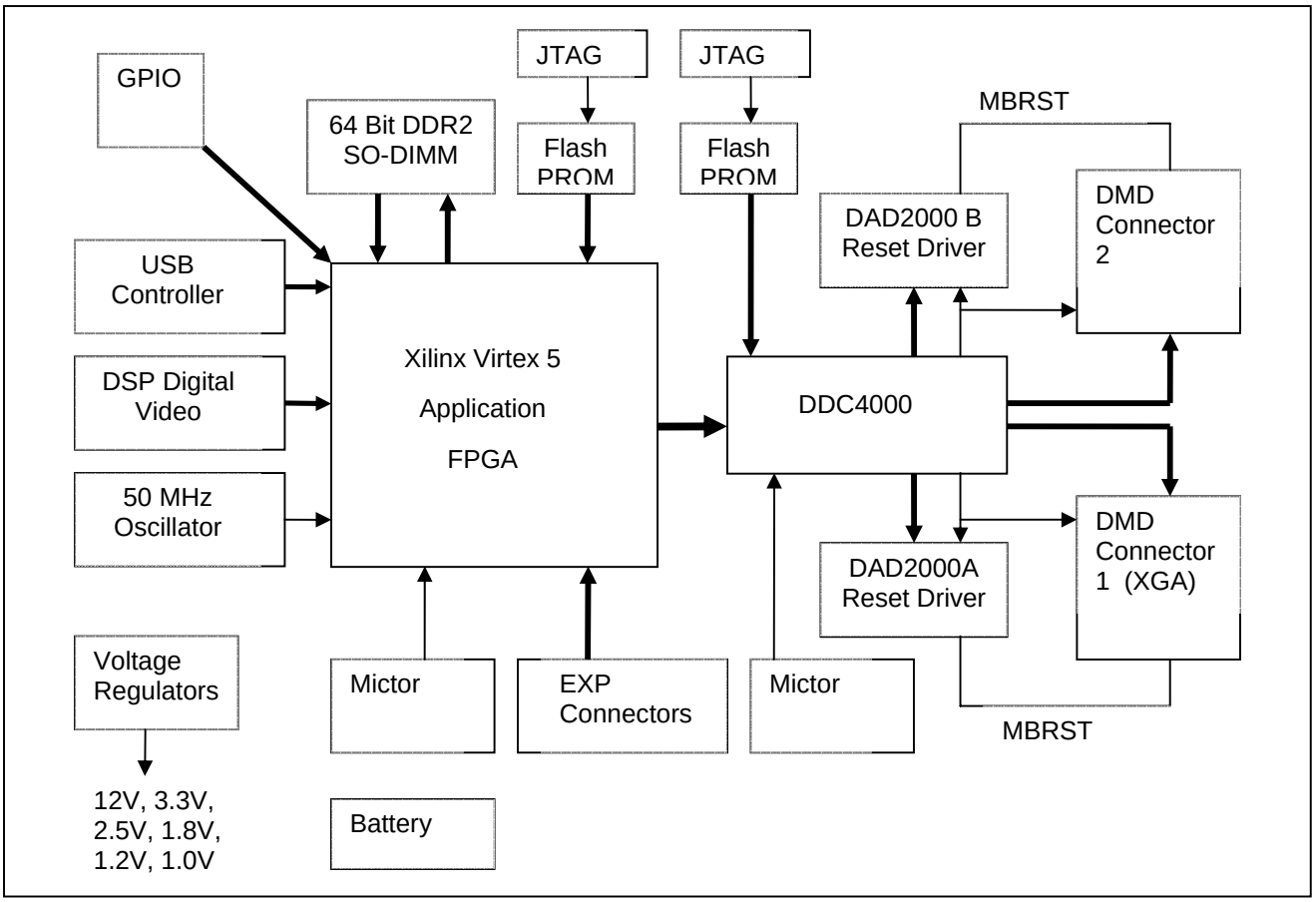


*Figure 3 D4000 Controller Board Key Components*

### 1.4.1 Xilinx Virtex 5 APPSFPGA

The Xilinx Virtex 5 LX Application FPGA (APPSFPGA) is used for development of interface and control solutions for the DMD. The APPSFPGA is connected to a number of I/O connectors, interface controllers and memory for use in prototyping a custom control solution prior to developing a custom board solution.

### 1.4.2 DDC4000 Controller

The DDC4000 chipset includes the DDC4000 controller which exposes a high-speed LVDS data and control interface for DMD control. This interface is connected to the APPSFPGA to support control from the APPSFPGA. The DDC4000 generates DMD and DAD2000 initialization and control signals in response to the inputs on the control interface.

For more information, refer to the DDC4000 Data Sheet TI DN 2509511.

### 1.4.3 DAD2000 Reset Drivers

Two DAD2000 reset drivers provide the high voltage power and reset driver functions for the DMD. One DAD2000 is required for XGA DMDs, two for 1080p DMD. J11 can be used to enable/disable the second DAD2000.

For more information on the DAD2000, refer to the DAD2000 data sheet TI DN 2506593.

### 1.4.4 50MHz Oscillator

The controller has a fixed 50 MHz 2.5V oscillator connected to the APPSFPGA for clock generation.

### 1.4.5 USB Controller

A Cypress 68013A USB controller is included for development of USB interface functions.

### 1.4.6 DDR2 SODIMM Connector

A 64 bit DDR2 SODIMM connector provides high speed memory connection to the APPSFPGA. Memory controller design for the APPSFPGA is not included. For a memory controller reference design visit www.xilinx.com .

### 1.4.7 Flash Configuration PROMs

For APPSFPGA configuration a Xilinx XCF16P Platform Flash PROM is provided. This PROM is pre-loaded with a test pattern generation program, however the customer can change the PROM programming as needed via JTAG.

The DDC4000 is configured at startup from a W25X80 serial flash PROM. The contents of this prom must not be altered.

### 1.4.8 Connectors

#### *1.4.8.1 DSP Digital Video*

The DSP digital video connector provides a digital video input to the APPSFPGA which is compatible with the Video Out connector of the Texas Instruments DaVinci™ DM644x EVM. No APPSFPGA or DM644x code is included for support of this connector. The connector may also be used as customer defined I/O.

#### *1.4.8.2 JTAG Headers*

The JTAG header ports provide a programming interface to the FPGAs and flash configuration PROMs. The JTAG header H1 accesses the Virtex 5 Application FPGA. The JTAG header H2 accesses the DDC4000 Lattice ECP2 and should not be used.

#### *1.4.8.3 Mictor Connectors*

The Mictor connector support connection of logic analyzer to APPSFPGA and Cypress 69013A signals for development support.

#### *1.4.8.4 DMD Connectors*

Two DMD connectors accept the DMD flex cable(s). Both cables are necessary to drive a 1080p DMD. One cable drive connected to J13 is used for XGA DMD.

#### *1.4.8.5 GPIO Connectors*

General purpose digital IO connectors.

### 1.4.9 Battery

A battery provides power for encryption security in Virtex 5. See Xilinx Virtex 5 data sheet for more detail.

### 1.4.10 Power Supplies

Onboard voltage regulation is provided for all required power supplies. This section lists controller voltage regulators and their purpose(s).

#### *1.4.10.1 Power Connector*

The D4000 controller board must be provided a 5 V 5 Amp supply.

#### *1.4.10.2 VREG 1.0V*

This delivers 3 Amps at 1.2 Volts as the Virtex 5 core supply.

#### *1.4.10.3 VREG 1.2V*

This delivers 3 Amps at 1.2 Volts as the Lattice 3 core supply.

#### *1.4.10.4 VREG 1.8V*

This delivers 3 Amps at 1.8 Volts for the DDR2 supply and FPGA I/O.

#### *1.4.10.5 VREG 2.5V*

This delivers 6 Amps at 2.5 Volts to supply the XCF16 FPGA I/O.

#### *1.4.10.6 VREG 3.3V*

This delivers 3 Amps at 3.3 Volts. Supply for DDC4000 prom and DMD.

#### *1.4.10.7 VREG 12V*

This delivers the DAD2000 12V 0.5 A supply.

## 2 Getting Started

The following steps should be followed in starting board operation using the default APPSFPGA code installed at the factory :

1.) Connect 5V, 5 A power supply to the supplied power cable. Connect the power cable to J12 with the power supply OFF.

2.) Confirm all SW2 switches are in the OFF position. Confirm all 5 H1 jumpers are in place. If using a 1080p DMD confirm J11 is installed.

3.) Connect the DMD to the board with the flex cable(s). One flex cable attached to J13 is used for XGA DMDs, two flex cables attached to J14 and J14 are used for 1080p DMD.

4.) Turn the power supply ON. D2 and D3 should briefly display red then green to indicate APPSFPGA and DDC4000 configuration. D8 should flash green at 1 Hz. D9 should display green. The DMD will repeatedly cycle through several test patterns.

To stop operation :

1.) Press SW2 to float the DMD, then turn power OFF.

# 3 User Connectors and I/O

*This section describes the use of each D4000 Controller Board external connector and provides pin out information. Figure 4 and Figure 5 show connector locations on the D4000 controller board.*

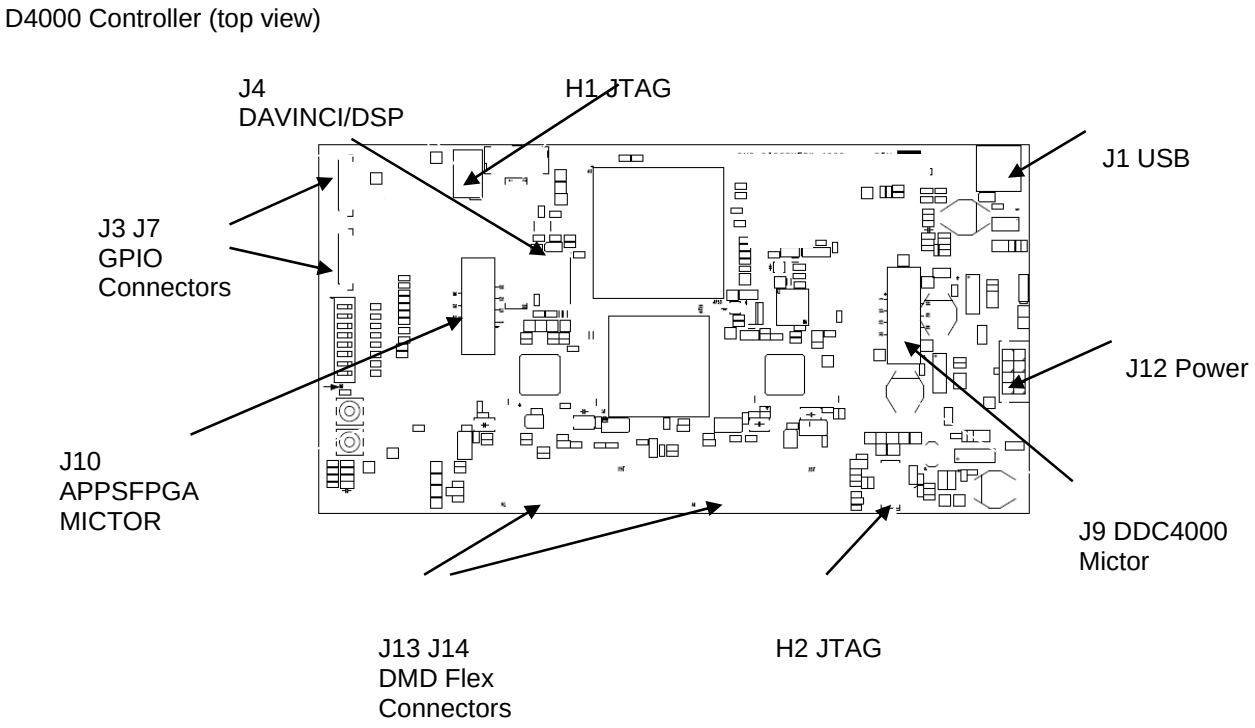


*Figure 4 D4000 Controller Connectors (top view)*

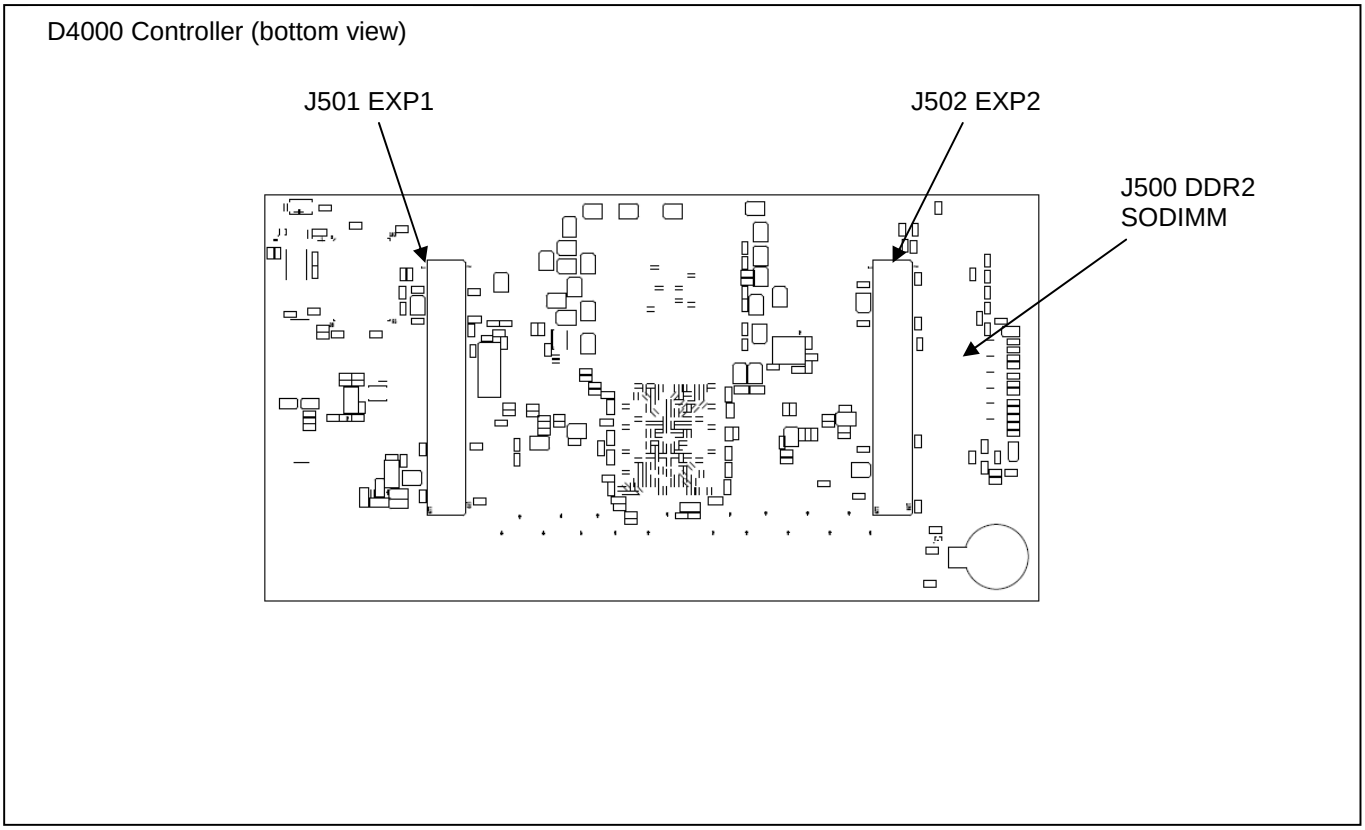


*Figure 5 D4000 Controller Connectors (bottom view)*

## *3.1 J1 USB Connector Pinout*

Connector J1 provides USB input to the controller board.

*Table 2 J18 USB*

| ***Pin number*** | ***Pin name*** | ***Pin number*** | ***Pin name*** |
|---|---|---|---|
| 1 | USB_5V | 2 | D- |
| 3 | D+ | 4 | NC |
| 5 | GND | | |

### *3.2 J3 USB GPIO*

Connector J3 provides 8 general purpose USB I/O pin connections to the USB Controller.

*Table 3 J3 USB GPIO*

| P1 Pin number | Pin name |
|---|---|
| 1 | 3.3V |
| 2 | USB_GPIO B7 |
| 3 | USB_GPIO B6 |
| 4 | USB_GPIO B5 |
| 5 | USB_GPIO B4 |
| 6 | USB_GPIO B3 |
| 7 | USB_GPIO B2 |
| 8 | USB_GPIO B1 |
| 9 | USB_GPIO B0 |
| 10 | GND |

### 3.3 J4 DAVINCI/DSP

The connector J4 provides DAVINCI/DSP video input access to the Virtex APPSFPGA.

*Table 4 J4 DAVINCI/DSP*

| J4 Pin number | Pin name | Virtex Pin Number | J4 Pin number | Pin name | Virtex Pin Number |
|---|---|---|---|---|---|
| 1 | DSP_GIO0 | K21 | 26 | GND | NC |
| 2 | DSP_GIO2 | J22 | 27 | DSP_YOUT0 | L23 |
| 3 | DSP_GIO3 | K17 | 28 | DSP_YOUT1 | AE23 |
| 4 | DSP_GIO5 | J19 | 29 | DSP_YOUT2 | AE22 |
| 5 | DSP_GIO6 | K16 | 30 | DSP_YOUT3 | AF23 |
| 6 | DSP_GIO38 | K18 | 31 | DSP_YOUT4 | AG23 |
| 7 | GND | NC | 32 | DSP_YOUT5 | AC15 |
| 8 | GND | NC | 33 | DSP_YOUT6 | AD15 |
| 9 | DSP_COUT0 | K14 | 34 | DSP_YOUT7 | AF15 |
| 10 | DSP_COUT1 | J12 | 35 | GND | NC |
| 11 | DSP_COUT2 | K13 | 36 | GND | NC |
| 12 | DSP_COUT3 | K12 | 37 | DSP_I2C_CLK | NC |
| 13 | DSP_COUT4 | L15 | 38 | DSP_SYS_RSTZ | AE14 |
| 14 | DSP_COUT5 | L14 | 39 | DSP_I2C_DATA | NC |
| 15 | DSP_COUT6 | L19 | 40 | GND | NC |
| 16 | DSP_COUT7 | L16 | 41 | VCC_1.8V | NC |
| 17 | GND | NC | 42 | VCC_1.8V | NC |
| 18 | GND | NC | 43 | GND | NC |
| 19 | DSP_VPBECLK | L20 | 44 | GND | NC |
| 20 | DSP_HSYNC | L21 | 45 | VCC_3.3V | NC |
| 21 | GND | NC | 46 | VCC_3.3V | NC |
| 22 | GND | NC | 47 | GND | NC |
| 23 | DSP_VCLK | K22 | 48 | GND | NC |
| 24 | DSP_VSYNC | K23 | 49 | VCC_5.0V | NC |
| 25 | GND | NC | 50 | VCC_5.0V | NC |

### 3.4 J7 GPIO_A Connector

Connector J7 provides 8 general purpose I/O pins to the Virtex 5 Application FPGA.

*Table 5 J7 GPIO_A Connector*

| P1 Pin number | Pin name | Virtex Pin Number |
|---|---|---|
| 1 | 2.5V | NC |
| 2 | GPIO A7 | AF20 |
| 3 | GPIO A6 | AF19 |
| 4 | GPIO A5 | AG12 |
| 5 | GPIO A4 | AH12 |
| 6 | GPIO A3 | AG16 |
| 7 | GPIO A2 | AG17 |
| 8 | GPIO A1 | AH19 |
| 9 | GPIO A0 | AG20 |
| 10 | GND | NC |

## 3.5 J9 DDC4000 Mictor Connector

J9 provides connection to the DDC4000 for a logic analyzer. This connector should not be used for normal development or operation.

*Table 6 J9 DDC4000 Mictor Connector*

| J9 Pin number | Pin name | DDC4000 Pin Number | J9 Pin Number | Pin Name | DDC4000 Pin Number |
|---|---|---|---|---|---|
| 1 | NC | NC | 2 | ECP2_M_TP0 | AD9 |
| 3 | GND | NC | 4 | ECP2_M_TP1 | AA11 |
| 5 | DDCSPARE0 | L7 | 6 | ECP2_M_TP2 | W11 |
| 7 | DDCSPARE1 | AC13 | 8 | ECP2_M_TP3 | AB26 |
| 9 | NC | NC | 10 | ECP2_M_TP4 | AB9 |
| 11 | NC | NC | 12 | ECP2_M_TP5 | AB11 |
| 13 | ECP2_M_TP31 | AA13 | 14 | ECP2_M_TP6 | AA10 |
| 15 | ECP2_M_TP3O | AB13 | 16 | ECP2_M_TP7 | AA12 |
| 17 | ECP2_M_TP29 | AD14 | 18 | ECP2_M_TP8 | Y11 |
| 19 | ECP2_M_TP28 | L5 | 20 | ECP2_M_TP9 | AB17 |
| 21 | ECP2_M_TP27 | AC14 | 22 | ECP2_M_TP10 | AA17 |
| 23 | ECP2_M_TP26 | AB15 | 24 | ECP2_M_TP11 | AA15 |
| 25 | ECP2_M_TP25 | H19 | 26 | ECP2_M_TP12 | AF12 |
| 27 | ECP2_M_TP24 | J18 | 28 | ECP2_M_TP13 | AE11 |
| 29 | ECP2_M_TP23 | H18 | 30 | ECP2_M_TP14 | AC9 |
| 31 | ECP2_M_TP22 | G15 | 32 | ECP2_M_TP15 | AF11 |
| 33 | ECP2_M_TP21 | G14 | 34 | ECP2_M_TP16 | AB12 |
| 35 | ECP2_M_TP20 | H17 | 36 | ECP2_M_TP17 | AA16 |
| 37 | ECP2_M_TP19 | G20 | 38 | ECP2_M_TP18 | AD13 |

## 3.6 J10 USB/APPSFPGA Mictor Connector

J10 is the Mictor connector for the USB controller and APPSFPGA Application FPGA. Signals from the USB or APPSFPGA are routed to the connector as selected by jumper J6. Refer to the Discovery™ 4000 Schematic for more information. Signals can be routed to the connector by HDL code and monitored with a logic analyzer to support development.

*Table 7 J10 USB/APPSFPGA Mictor Connector*

| Pin number | Pin name | APPSFPGA Pin Number | Pin Number | Pin Name | APPSFPGA Pin Number |
|---|---|---|---|---|---|
| 1 | NC | NC | 2 | NC | NC |
| 3 | GND | NC | 4 | D4000_I2C_CLK | P29 |
| 5 | USB_IF_CLK/ TEST_CLK_0 | N29 | 6 | D4000_I2C_DATA | U28 |
| 7 | USB_FDO/ TST_HDR_BY0_0 | H29 | 8 | GPIFADR0/ TST_HDR_BY2_0 | K31 |
| 9 | USB_FD1/ TST_HDR_BY0_1 | H30 | 10 | GPIFADR1/ TST_HDR_BY2_1 | L31 |
| 11 | USB_FD2/ TST_HDR_BY0_2 | J31 | 12 | GPIFADR2/ TST_HDR_BY2_2 | P31 |
| 13 | USB_FD3/ TST_HDR_BY0_3 | G30 | 14 | GPIFADR3/ TST_HDR_BY2_3 | P30 |
| 15 | USB_FD4/ TST_HDR_BY0_4 | J30 | 16 | GPIFADR4/ TST_HDR_BY2_4 | N30 |
| 17 | USB_FD5/ TST_HDR_BY0_5 | G31 | 18 | GPIFADR5/ TST_HDR_BY2_5 | M31 |
| 19 | USB_FD6/ TST_HDR_BY0_6 | J29 | 20 | GPIFADR6/ TST_HDR_BY2_6 | R28 |
| 21 | USB_FD7/ TST_HDR_BY0_7 | F29 | 22 | GPIFADR7/ TST_HDR_BY2_7 | R29 |
| 23 | USB_FD8/ TST_HDR_BY1_0 | K29 | 24 | GPIFADR8/ TST_HDR_BY3_0 | T31 |
| 25 | USB_FD9/ TST_HDR_BY1_1 | F30 | 26 | USB_CTRL0/ TST_HDR_BY3_1 | R31 |
| 27 | USB_FD1O/ TST_HDR_BY1_2 | L30 | 28 | USB_CTRL1/ TST_HDR_BY3_2 | U30 |
| 29 | USB_FD11/ TST_HDR_BY1_3 | F31 | 30 | USB_CTRL2/ TST_HDR_BY3_3 | T30 |
| 31 | USB_FD12/ TST_HDR_BY1_4 | L29 | 32 | USB_CTRL3/ TST_HDR_BY3_4 | T28 |
| 33 | USB_FD13/ TST_HDR_BY1_5 | E29 | 34 | USB_FPGA_RESET/ TST_HDR_BY3_5 | T29 |
| 35 | USB_FD14/ TST_HDR_BY1_6 | E31 | 36 | USB_INT5/ TST_HDR_BY3_6 | U27 |
| 37 | USB_FD15/ TST_HDR_BY1_7 | M30 | 38 | NC | NC |

## 3.7 J13 and J14 DMD Flex Connector

Connectors J13 and J14 provide control and data signals to the DMD flex connectors. These connectors are used for DMD connections.

## 3.8 J500 DDR2 SODIMM Connector

Connector J500 provides a DDR2 SODIMM memory socket. No memory module is included. Memory controller design for the APPSFPGA is not included. For a memory controller reference design visit www.xilinx.com .

*Table 8 J500 DDR2 SODIMM Connector*

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| 1 | VCC_VREF | 2 | GND | 3 | GND | 4 | DDR2_D4 |
| 5 | DDR2_D0 | 6 | DDR2_D5 | 7 | DDR2_D1 | 8 | GND |
| 9 | GND | 10 | DDR2_DM0 | 11 | DDR2_DQS0_N | 12 | GND |
| 13 | DDR2_DQS0_P | 14 | DDR2_D6 | 15 | GND | 16 | DDR2_D7 |
| 17 | DDR2_D2 | 18 | GND | 19 | DDR2_D3 | 20 | DDR2_D12 |
| 21 | GND | 22 | DDR2_D13 | 23 | DDR2_D8 | 24 | GND |
| 25 | DDR2_D9 | 26 | DDR2_DM1 | 27 | GND | 28 | GND |
| 29 | DDR2_DOS1_N | 30 | DDR2_CK0_P | 31 | DDR2_DOS1_P | 32 | DDR2_CK0_N |
| 33 | GND | 34 | GND | 35 | DDR2_D10 | 36 | DDR2_D14 |
| 37 | DDR2_D11 | 38 | DDR2_D15 | 39 | GND | 40 | GND |
| 41 | GND | 42 | GND | 43 | DDR2_D16 | 44 | DDR2_D20 |
| 45 | DDR2_D17 | 46 | DDR2_D21 | 47 | GND | 48 | GND |
| 49 | DDR2_DQS2_N | 50 | NC | 51 | DDR2_DQS2_P | 52 | DDR2_DM2 |
| 53 | GND | 54 | GND | 55 | DDR2_D18 | 56 | DDR2_D22 |
| 57 | DDR2_D19 | 58 | DDR2_D23 | 59 | GND | 60 | GND |
| 61 | DDR2_D24 | 62 | DDR2_D28 | 63 | DDR2_D25 | 64 | DDR2_D29 |
| 65 | GND | 66 | GND | 67 | DDR2_DM3 | 68 | DDR2_DQS3_N |
| 69 | NC | 70 | DDR2_DQS3_P | 71 | GND | 72 | GND |
| 73 | DDR2_D26 | 74 | DDR2_D30 | 75 | DDR2_D27 | 76 | DDR2_D31 |
| 77 | GND | 78 | GND | 79 | DDR2_CKE0 | 80 | DDR2_CKE0 |
| 81 | 1.8V | 82 | 1.8V | 83 | NC | 84 | NC |
| 85 | DDR2_BA2 | 86 | NC | 87 | 1.8V | 88 | 1.8V |

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| 89 | DDR2_A12 | 90 | DDR2_A11 | 91 | DDR2_A9 | 92 | DDR2_A7 |
| 93 | DDR2_A8 | 94 | DDR2_A6 | 95 | 1.8V | 96 | 1.8V |
| 97 | DDR2_A5 | 98 | DDR2_A4 | 99 | DDR2_A3 | 100 | DDR2_A2 |
| 101 | DDR2_A1 | 102 | DDR2_A0 | 103 | 1.8V | 104 | 1.8V |
| 105 | DDR2_A10 | 106 | DDR2_BA1 | 107 | DDR2_BA0 | 108 | DDR2_RAS_B |
| 109 | DDR2_WE_B | 110 | DDR2_CS0_B | 111 | 1.8V | 112 | 1.8V |
| 113 | DDR2_CAS_B | 114 | DDR2_ODT0 | 115 | DDR2_CS1_B | 116 | DDR2_A13 |
| 117 | 1.8V | 118 | 1.8V | 119 | DDR2_ODT1 | 120 | NC |
| 121 | GND | 122 | GND | 123 | DDR2_D32 | 124 | DDR2_D36 |
| 125 | DDR2_D33 | 126 | DDR2_D37 | 127 | GND | 128 | GND |
| 129 | DDR2_DQS4_N | 130 | DDR2_DDM4 | 131 | DDR2_DQS4_P | 132 | GND |
| 133 | GND | 134 | DDR2_D38 | 135 | DDR2_D34 | 136 | DDR2_D30 |
| 137 | DDR2_D35 | 138 | GND | 139 | GND | 140 | DDR2_D44 |
| 141 | DDR2_D40 | 142 | DDR2_D44 | 143 | DDR2_D41 | 144 | GND |
| 145 | GND | 146 | DDR2_DQS5_N | 147 | DDR2_DM5 | 148 | DDR2_DQS5_P |
| 149 | GND | 150 | GND | 151 | DDR2_D42 | 152 | DDR2_D46 |
| 153 | DDR2_D43 | 154 | DDR2_D47 | 155 | GND | 156 | GND |
| 157 | DDR2_D48 | 158 | DDR2_D52 | 159 | DDR2_D49 | 160 | DDR2_D53 |
| 161 | GND | 162 | GND | 163 | NC | 164 | DDR2_CK1_P |
| 165 | GND | 166 | DDR2_CK1_N | 167 | DDR2_DQ56_N | 168 | GND |
| 169 | DDR2_DQ56_P | 170 | DDR2_DM6 | 171 | GND | 172 | GND |
| 173 | DDR2_D50 | 174 | DDR2_D54 | 175 | DDR2_D51 | 176 | DDR2_D55 |
| 177 | GND | 178 | GND | 179 | DDR2_D56 | 180 | DDR2_D60 |
| 181 | DDR2_D57 | 182 | DDR2_D61 | 183 | GND | 184 | GND |
| 185 | DDR2_DM7 | 186 | DDR2_DQS7_N | 187 | GND | 188 | DDR2_DQS7_P |
| 189 | DDR2_D58 | 190 | GND | 191 | DDR2_D59 | 192 | DDR2_D62 |
| 193 | GND | 194 | DDR2_D63 | 195 | DDR2_SDA | 196 | GND |
| 197 | DDR2_SDL | 198 | GND | 199 | 1.8V | 200 | GND |

## 3.9 J501, J502 EXP Connectors

J501 and J502 provide connections compatible with the Avnet EXP Bus Specification. Refer to www.em.avnet.com/exp for more information. J501 and J502 may also be used as high speed interface connectors for accessory boards. The D4000 controller board routes some of the single ended signals as differential pairs to support a full 64 bit LVDS data bus. This routing may interfere with the use some of the EXP single ended signals as noted in the table footnote.

*Table 9 J501, J502 EXP Connectors*

| J501 Pin Number | Single Ended Signal Name | Differential Pair Name | Virtex5 Pin Number | J501 Pin Number | Single Ended Signal Name | Differential Pair Name | Virtex5 Pin Number |
|---|---|---|---|---|---|---|---|
| **1** | **EXP1_SE_IO_1** | | **A33** | **2** | **EXP1_SE_IO_0** | | **C34** |
| 3 | EXP1_SE_IO_3 | | B32 | 4 | EXP1_SE_IO_2 | | D32 |
| 7 | EXP1_SE_IO_5 | | B33 | 8 | EXP1_SE_IO_4 | | D34 |
| 9 | EXP1_SE_IO_7 | | C32 | 10 | EXP1_SE_IO_6 | | E34 |
| 13 | EXP1_SE_IO_9 | | H32 | 14 | EXP1_SE_IO_8 | | G32 |
| 15 | EXP1_SE_IO_11 | | C33 | 16 | EXP1_SE_IO_10 | | F33 |
| 19 | EXP1_SE_IO_13* | EXP1_DIFF_23_P | K33 | 20 | EXP1_SE_IO_12* | EXP1_DIFF_22 | G33 |
| 21 | EXP1_SE_IO_15* | EXP1_DIFF_23_N | K32 | 22 | EXP1_SE_IO_14* | EXP1_DIFF_22 | F34 |
| 25 | EXP1_SE_IO_17* | EXP1_DIFF_25_P | P34 | 26 | EXP1_SE_IO_16* | EXP1_DIFF_24 | H34 |
| 27 | EXP1_SE_IO_19* | EXP1_DIFF_25_N | N34 | 28 | EXP1_SE_IO_18* | EXP1_DIFF_24 | J34 |
| 31 | EXP1_SE_IO_21* | EXP1_DIFF_27_P | N33 | 32 | EXP1_SE_IO_20* | EXP1_DIFF_26 | L34 |
| 33 | EXP1_SE_IO_23* | EXP1_DIFF_27_N | M33 | 34 | EXP1_SE_IO_22* | EXP1_DIFF_26 | K34 |
| 37 | EXP1_SE_IO_25* | EXP1_DIFF_29_P | L33 | 38 | EXP1_SE_IO_24* | EXP1_DIFF_28 | J32 |
| 39 | EXP1_SE_IO_27* | EXP1_DIFF_29_N | M32 | 40 | EXP1_SE_IO_26* | EXP1_DIFF_28 | H33 |
| 41 | EXP1_SE_IO_28 | | E32 | 42 | | EXP1_DIFF_CLK_IN_DPP | H19 |
| 43 | EXP1_SE_CLK_IN | | J20 | 44 | | EXP1_DIFF_CLK_IN_DPN | H20 |
| 47 | EXP1_SE_IO_29 | | E33 | 48 | EXP1_SE_IO_30* | EXP1_DIFF_30_P | R33 |
| 49 | EXP1_SE_CLK_OUT | | J21 | 50 | EXP1_SE_IO_3* | EXP1_DIFF_30_N | R32 |
| 53 | | EXP1_DIFF_21_P | P32 | 54 | | EXP1_DIFF_20_P | AC32 |
| 55 | | EXP1_DIFF_21_N | N32 | 56 | | EXP1_DIFF_20_N | AB32 |
| 59 | EXP1_SE_IO_32* | EXP1_DIFF_31_P | T33 | 60 | | EXP1_DIFF_18_P | AF34 |
| 61 | EXP1_SE_IO_33* | EXP1_DIFF_31_N | R34 | 62 | | EXP1_DIFF_18_N | AE34 |
| 65 | | EXP1_DIFF_19_P | AG32 | 66 | | EXP1_DIFF_16_P | U33 |
| 67 | | EXP1_DIFF_19_N | AH32 | 68 | | EXP1_DIFF_16_N | T34 |
| 71 | | EXP1_DIFF_17_P | AJ32 | 72 | | EXP1_DIFF_CLK_OUT_P | U3 |
| 73 | | EXP1_DIFF_17_N | AK32 | 74 | | EXP1_DIFF_CLK_OUT_N | U2 |
| 77 | | EXP1_DIFF_15_P | W34 | 78 | | EXP1_DIFF_14_P | V33 |
| 79 | | EXP1_DIFF_15_N | V34 | 80 | | EXP1_DIFF_14_N | V32 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 81 | | EXP1_DIFF_13_P | AA34 | 82 | | EXP1_DIFF_12_P | AD32 |
| 83 | | EXP1_DIFF_13_N | Y34 | 84 | | EXP1_DIFF_12_N | AE32 |
| 87 | | EXP1_DIFF_11_P | Y32 | 88 | | EXP1_DIFF_10_P | AL34 |
| 89 | | EXP1_DIFF_11_N | W32 | 90 | | EXP1_DIFF_10_N | AL33 |
| 93 | | EXP1_DIFF_9_P | AA33 | 94 | | EXP1_DIFF_8_P | AK34 |
| 95 | | EXP1_DIFF_9_N | Y33 | 96 | | EXP1_DIFF_8_N | AK33 |
| 99 | | EXP1_DIFF_7_P | AC33 | 100 | | EXP1_DIFF_6_P | AF33 |
| 101 | | EXP1_DIFF_7_N | AB33 | 102 | | EXP1_DIFF_6_N | AE33 |
| 105 | | EXP1_DIFF_5_P | AC34 | 106 | | EXP1_DIFF_4_P | AH34 |
| 107 | | EXP1_DIFF_5_N | AD34 | 108 | | EXP1_DIFF_4_N | AJ34 |
| 111 | | EXP1_DIFF_3_P | AM33 | 112 | | EXP1_DIFF_2_P | AG33 |
| 113 | | EXP1_DIFF_3_N | AM32 | 114 | | EXP1_DIFF_2_N | AH33 |
| 117 | | EXP1_DIFF_1_P | AN34 | 118 | | EXP1_DIFF_0_P | AN32 |
| 119 | | EXP1_DIFF_1_N | AN33 | 120 | | EXP1_DIFF_0_N | AP32 |

** Single ended IO with shared differential pairs, should only be slow switching signals, or only one side of the pair should be used.*

| J502 Pin Number | Power Connection |
|---|---|
| 5,6,11,12,17,18,23,24,29,30,35,36 | VCC_2P5V |
| 45,46,41,52,57,58,63,64,69,70,75,76,121,122,<br>124,125,126,127,128,129,130,131,132 | Ground |
| 85,86,91,92,97,98,103,104,109,110,115,116 | VCC_3P3V |

| J502 Pin Number | Single Ended Signal Nam | Differential Pair Name | Virtex5 Pin Number | J502 Pin Number | Single Ended Signal Name | Differential Pair Name | Virtex5 Pin Number |
|---|---|---|---|---|---|---|---|
| 1 | EXP2_SE_IO_1 | | D1 | 2 | EXP2_SE_IO_0 | | B3 |
| 3 | EXP2_SE_IO_3 | | D2 | 4 | EXP2_SE_IO_2 | | B1 |
| 7 | EXP2_SE_IO_5 | | J2 | 8 | EXP2_SE_IO_4 | | B2 |
| 9 | EXP2_SE_IO_7 | | J1 | 10 | EXP2_SE_IO_6 | | A3 |
| 13 | EXP9_SE_IO_9 | | K1 | 14 | EXP2_SE_IO_8 | | C2 |
| 15 | EXP2_SE_IO_11 | | K2 | 16 | EXP2_SE_IO_10 | | C3 |
| 19 | EXP2_SE_IO_13* | EXP2_DIFF_23_P | H2 | 20 | EXP2_SE_IO_12* | EXP2_DIFF_22 | E2 |
| 21 | EXP2_SE_IO_15* | EXP2_DIFF_23_N | H3 | 22 | EXP2_SE_IO_14* | EXP2_DIFF_22 | E1 |
| 25 | EXP2_SE_IO_17* | EXP2_DIFF_25_P | P2 | 26 | EXP2_SE_IO_16* | EXP2_DIFF_24 | E3 |
| 27 | EXP2_SE_IO_19* | EXP2_DIFF_25_N | R3 | 28 | EXP2_SE_IO_18* | EXP2_DIFF_24 | F3 |
| 31 | EXP2_SE_IO_21* | EXP2_DIFF_27_P | T1 | 32 | EXP2_SE_IO_20* | EXP2_DIFF_26 | F1 |
| 33 | EXP2_SE_IO_23* | EXP2_DIFF_27_N | R1 | 34 | EXP2_SE_IO_22* | EXP2_DIFF_26 | G1 |
| 37 | EXP2_SE_IO_25* | EXP2_DIFF_29_P | K3 | 38 | EXP2_SE_IO_24* | EXP2_DIFF_28 | G3 |
| 39 | EXP2_SE_IO_27* | EXP2_DIFF_29_N | L3 | 40 | EXP2_SE_IO_26* | EXP2_DIFF_28 | G2 |
| 41 | EXP2_SE_IO_28 | | Y2 | 42 | | EXP2_DIFF_CLK_IN_DPP | H18 |
| 43 | EXP2_SE_CLK_IN | | J16 | 44 | | EXP2_DIFF_CLK_IN_DPN | J17 |
| 47 | EXP2_SE_IO_29 | | Y3 | 48 | EXP2_SE_IO_30* | EXP2_DIFF_30_P | N2 |
| 49 | EXP2_SE_CLK_OUT | | J15 | 50 | EXP2_SE_IO_31 | EXP2_DIFF_30_ | M2 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | N | |
| 53 | | EXP2_DIFF_21_P | M3 | 54 | | EXP2_DIFF_20_P | M1 |
| 55 | | EXP2_DIFF_21_N | N3 | 56 | | EXP2_DIFF_20_N | L1 |
| 59 | EXP2_SE_IO_32* | EXP2_DIFF_31_P | P1 | 60 | | EXP2_DIFF_18_P | V4 |
| 61 | EXP2_SE_IO_33* | EXP2_DIFF_31_N | R2 | 62 | | EXP2_DIFF_18_N | V3 |
| 65 | | EXP2_DIFF_19_P | U3 | 66 | | EXP2_DIFF_16_P | W1 |
| 67 | | EXP2_DIFF_19_N | T3 | 68 | | EXP2_DIFF_16_N | V2 |
| 71 | | EXP2_DIFF_17_P | U1 | 72 | | EXP2_DIFF_CLK_OUT_P | AC3 |
| 73 | | EXP2_DIFF_17_N | U2 | 74 | | EXP2_DIFF_CLK_OUT_N | AB2 |
| 77 | | EXP2_DIFF_15_P | W2 | 78 | | EXP2_DIFF_14_P | AB3 |
| 79 | | EXP2_DIFF_15_N | Y1 | 80 | | EXP2_DIFF_14_N | AA3 |
| 81 | | EXP2_DIFF_13_P | AF1 | 82 | | EXP2_DIFF_12_P | AG1 |
| 83 | | EXP2_DIFF_13_N | AE1 | 84 | | EXP2_DIFF_12_N | AG2 |
| 87 | | EXP2_DIFF_11_P | AF3 | 88 | | EXP2_DIFF_10_P | AE2 |
| 89 | | EXP2_DIFF_11_N | AE3 | 90 | | EXP2_DIFF_10_N | AD2 |
| 93 | | EXP2_DIFF_9_P | AH2 | 94 | | EXP2_DIFF_8_P | AB1 |
| 95 | | EXP2_DIFF_9_N | AJ2 | 96 | | EXP2_DIFF_8_N | AA1 |
| 99 | | EXP2_DIFF_7_P | AK2 | 100 | | EXP2_DIFF_6_P | AG3 |
| 101 | | EXP2_DIFF_7_N | AK3 | 102 | | EXP2_DIFF_6_N | AH3 |
| 105 | | EXP2_DIFF_5_P | AJ1 | 106 | | EXP2_DIFF_4_P | AC2 |
| 107 | | EXP2_DIFF_5_N | AK1 | 108 | | EXP2_DIFF_4_N | AD1 |
| 111 | | EXP2_DIFF_3_P | AM3 | 112 | | EXP2_DIFF_2_P | AN2 |
| 113 | | EXP2_DIFF_3_N | AN3 | 114 | | EXP2_DIFF_2_N | AP2 |
| 117 | | EXP2_DIFF_1_P | AL1 | 118 | | EXP2_DIFF_0_P | AM2 |
| 119 | | EXP2_DIFF_1_N | AM1 | 120 | | EXP2_DIFF_0_N | AL3 |

** Single ended IO with shared differential pairs, should only be slow switching signals, or only one side of the pair should be used.*

| J502 Pin Number | Power Connection |
|---|---|
| 5,6,11,12,17,18,23,24,29,30,35,36 | VCC_2P5V |
| 45,46,41,52,57,58,63,64,69,70,75,76,121,122,<br>124,125,126,127,128,129,130,131,132 | Ground |
| 85,86,91,92,97,98,103,104,109,110,115,116 | VCC_3P3V |

## 3.10 H1 Xilinx APPSFPGA JTAG header

Provides direct connection for a Xilinx JTAG programming cable. Xilinx Model DLC9G is recommended. Visit www.xilinx.com for more information.

*Table 10 H1 Xilinx APPSFPGA JTAG Header*

| Pin number | Pin name |
|---|---|
| 1,3,5,7,9,11,13 | GND |
| 2 | P2P5V |
| 4 | TMS |
| 6 | TCK |
| 8 | TDO |
| 10 | TDI |
| 12,14 | NC |

## 3.11 H2 DDC4000 JTAG Header

Provides direct connection for a Lattice JTAG programming cable. This connector will not be used for normal development or operation.

*Table 11 H2 DDC4000 JTAG Header*

| Pin number | Pin name |
|---|---|
| 1,3,5,7,9,11,13 | GND |
| 2 | P2P5V |
| 4 | TMS |
| 6 | TCK |
| 8 | TDO |
| 10 | TDI |
| 12,14 | NC |

# 4 Configuration Jumpers

*This section describes the D4000 Controller Board configuration jumpers. Figure 6 shows jumperr locations on the D4000 controller board.*

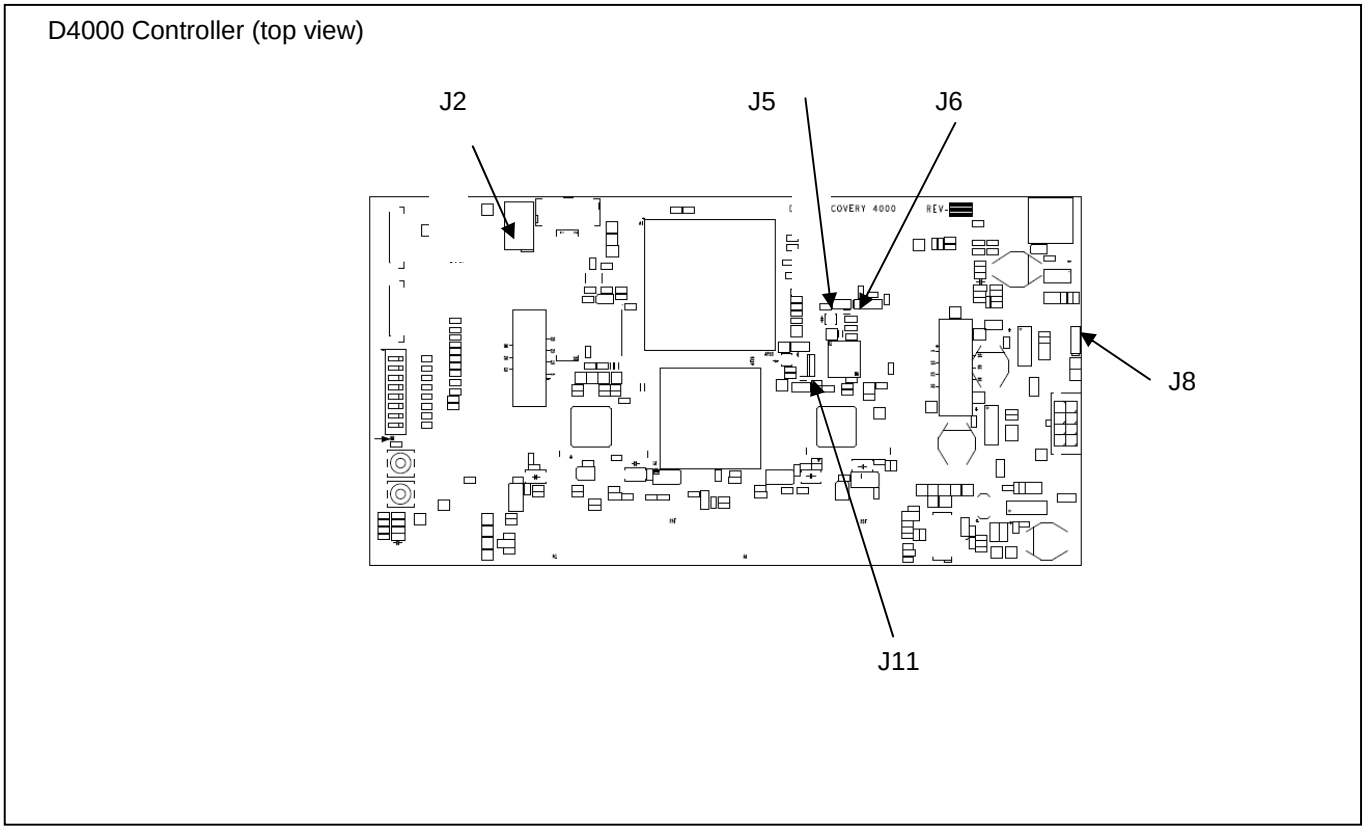


*Figure 6 D4000 Controller Configuration Jumpers*

## *4.1 J2 – EXP Voltage Select*

J2 – Used to select either 2.5V or 3.3V voltage supplies for the EXP bus FPGA banks. This setting should match the I/O voltage required by any board attached to the EXP connectors.

| Position | Bank Voltage |
|---|---|
| 1-2 | 3.3V |
| 2-3 | 2.5V |

## 4.2 J5 – Application FPGA Revision Select

J5 – Used to select the revision of firmware in loaded from the PROM to the APPSFPGA.

| Jumper Position | Revision Version |
|---|---|
| 0-1 | 0 |
| 1-2 | 1 |

## 4.3 J11 – DAD2000 B Output Enable

J11 – Used to enable the outputs for DAD2000 B. This needs to be enabled only if using the 1080P DMD, otherwise this can be disabled.

| Jumper Position | DAD2000 B Outputs |
|---|---|
| 0-1 | Disabled |
| 1-2 | Enabled |

## 4.4 J6 – Shared USB signal disabled

J6 – Used to connect or disconnect the USB signals that are shared between the USB/APPSFPGA Mictor Connector J10. This could be useful to isolate test signals from the FPGA to the Mictor connector.

| Jumper Position | USB Signals |
|---|---|
| 0-1 | Disconnected from FPGA |
| 1-2 | Connected to FPGA |
| 2-3 | Automatically connect USB signals to FPGA when USB is connected to host PC |

## 4.5 J8 – USB EEPROM Programming Header

J8 – Used to temporally disconnect the USB EEPROM from the device so the device can load its internal boot loader rather than any code in the EEPROM. Install J8 for Cypress internal boot loader.

## 4.6 H1 – JTAG interface Virtex 5

H1 Provides a JTAG interface to program Virtex 5 Application FPGA and its associated PROM.

*Table 12 H1 APPSFPGA JTAG header*

| Pin number | Pin name |
|---|---|
| 1,3,5,7,9,11,13 | GND |
| 2 | P2P5V |
| 4 | TMS |
| 6 | TCK |
| 8 | TDO |
| 10 | TDI |
| 12,14 | NC |

## 4.7 H2– JTAG interface Lattice ECP-2

H2 Provides a JTAG interface to program the Lattice ECP2 FPGA and its associated PROM.

*Table 13 H2 ECP2 JTAG header*

| Pin number | Pin name |
|---|---|
| 1,3,5,7,9,11,13 | GND |
| 2 | P2P5V |
| 4 | TMS |
| 6 | TCK |
| 8 | TDO |
| 10 | TDI |
| 12,14 | NC |

# 5 Switches

This section defines the function of D4000 switches.

## 5.1 Dipswitches – SW1

Functionality defined by APPSFPGA programming. In default test pattern code:

*Table 14 Dipswitch Assignments*

| Switch Number | Effect |
|---|---|
| 1 | ON = float – float all mirrors |
| 2 | ON = counter halt – stop counter, this will freeze the image on the DMD |
| 3 | ON = complement data – causes DDC 4000 to complement all data it receives |
| 4 | ON = north/south flip – causes the DDC 4000 to reverse order of row loading, effectively flipping the image |
| 6 and 5 | Dictates the type of reset being used (where switch 6 is the MSB and ON = 1):<br>00 : single block phased reset<br>01 : dual block phased reset<br>10 : global reset<br>11 : quad block phased reset |
| 7 | ON = Row Address Mode |
| 8 | ON = WDT Enable, disables other resets |

## 5.2 Push Button Momentary Switch – SW2

Functionality defined by APPSFPGA. This switch is used for PWR_FLOAT in the default code.

## 5.3 Push Button Momentary Switch – SW3

Functionality defined by APPSFPGA. This switch is used for reset in the default code.

# 6 Power and Status LEDs

This chapter provides an illustration of indicators used to verify that the DDC4000 Controller Board is functioning properly. Figure 7 shows the controller board indicator locations.

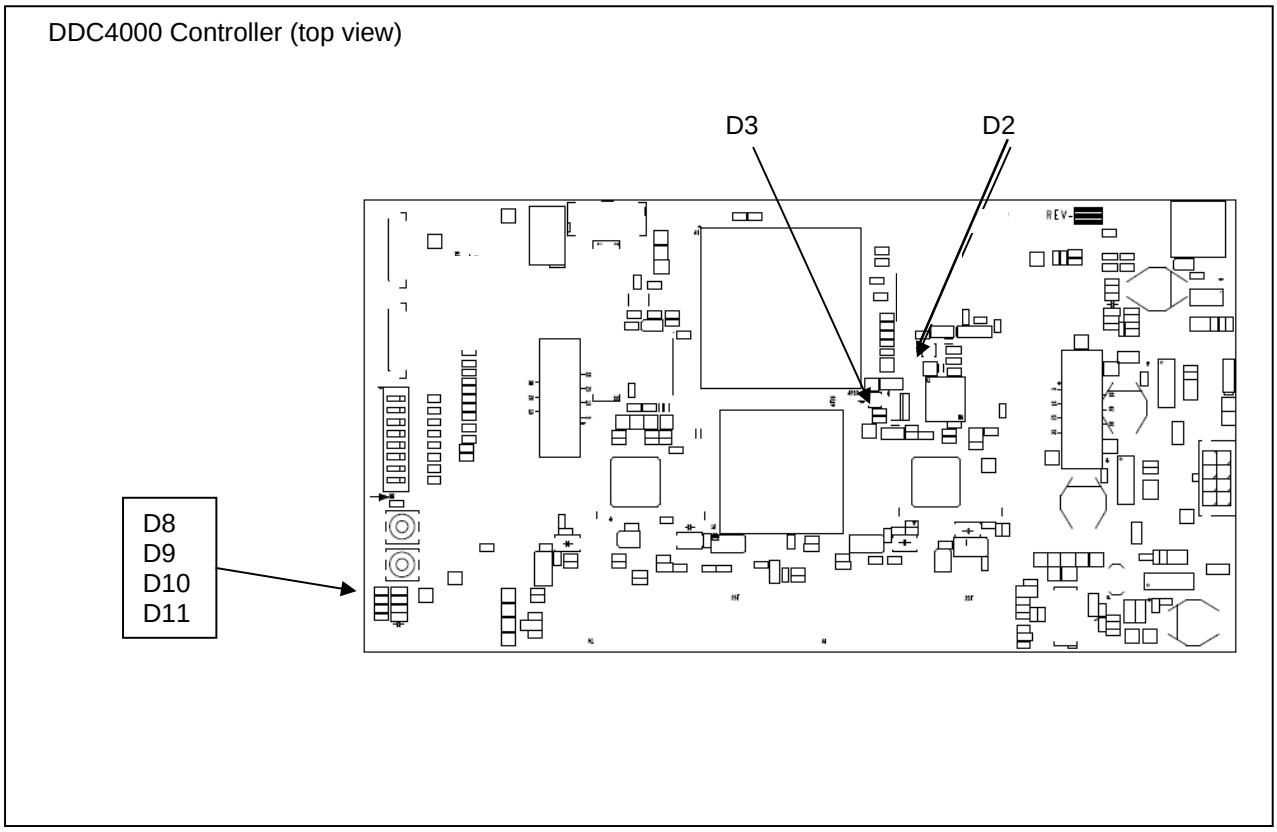


*Figure 7 DDC4000 Controller Board Indicators*

## 6.1 D2 – APPSFPGA done

D2 is a two color LED, red and green.

The red side is turned on when the APPSFPGA DONE pin is low, not DONE. Red turns off when the DONE pin goes high indicating the APPSFPGA completed programming successfully. To further assure the APPSFPGA is up and running, the green LED is turned on by internal logic once all pins are turned on. This logic is to be defined by the application, although it could be a DCM lock monitor or a 'heart beat' indicating clocks are operating, the default load drives this with a simple high to turn the green LED on.

## 6.2 D3 – DDC4000 done

D3 is a two color LED, red and green.

The red side is turned on when the DDC4000 DONE pin is low, not DONE. Red turns off when the DONE pin goes high indicating the DDC4000 completed programming successfully. Green turns on when I/O pins are enabled after programming.

### *6.3 D8 – DDC_LED0*

D8 – DDC_LED0 – Status LED for the DDC4000. See the DDC4000 data sheet for more details.

### *6.4 D9 – DDC_LED1*

D9 – DDC_LED1 – Status LED for the DDC4000. See the DDC4000 data sheet for more details.

### *6.5 D10 – VLED0*

D10 – VLED0 – This logic is to be defined by the APPSFPGA application. Drive low to turn on the led. Drive high to turn off the led.

### *6.6 D11 – VLED1*

D11 – VLED1 -This logic is to be defined by the APPSFPGA application. Drive low to turn on the led. Drive high to turn off the led.

# 7 Test Points

This chapter defines the location of on-board test points.

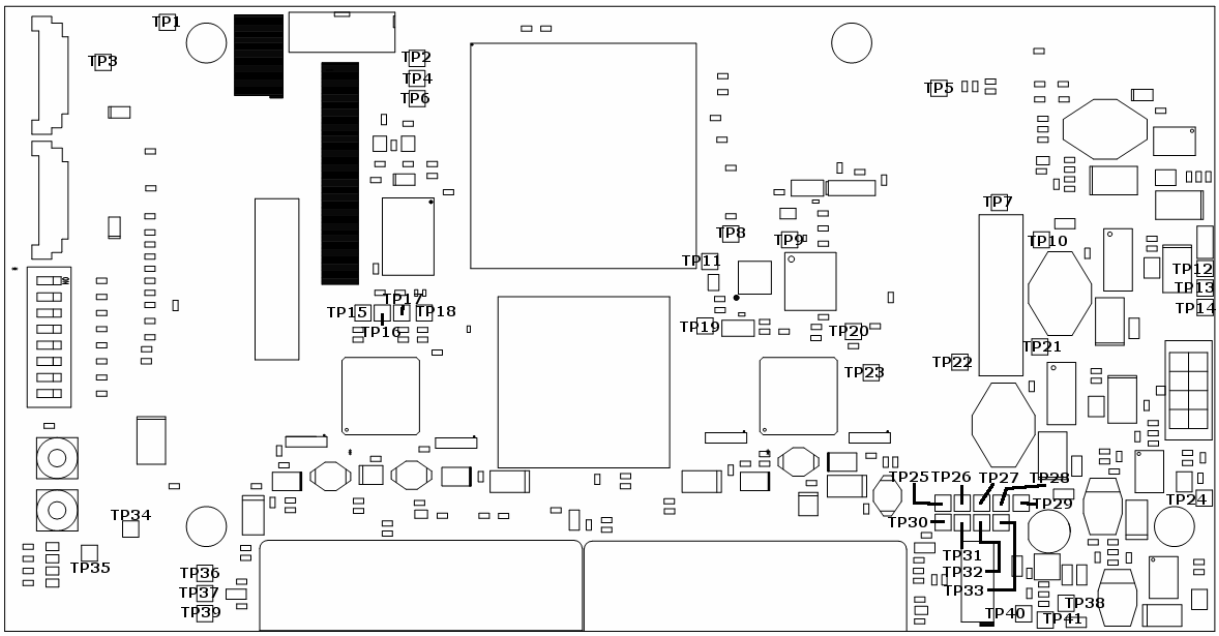


*Figure 8 Test Point Locations*

*Table 15 Test Points*

| Test Pont | Net Name | Test Point | Net Name |
|---|---|---|---|
| TP1 | GROUND | TP2 | V5_DXP |
| TP3 | VCC_VREF | TP4 | V5_DXN |
| TP5 | GROUND | TP6 | RESET |
| TP7 | 2.5V TEST | TP8 | ECP2_CCLK |
| TP9 | SCPDO | TP10 | 3.3V TEST |
| TP11 | ECP2_SISPI | TP12 | USB_EA |
| TP13 | VCC_3P3V | TP14 | VCC_2P5V |

| | | | |
|---|---|---|---|
| TP15 | MBRST1_8 | TP16 | DAD_A_ IRQZ |
| TP17 | ECP2_SPIDO | TP18 | ECP2_CS# |
| TP19 | SCPCLK | TP20 | DAD_B_ IRQZ |
| TP21 | 1.8V TEST | TP22 | PWRGD |
| TP23 | MBRST2_0 | TP24 | 1.2V TEST |
| TP25 | SCPDI | TP26 | DMDSPARE2 |
| TP27 | MBRST2_8 | TP28 | VCC_12V |
| TP29 | GROUND | TP30 | VCC_1P2V |
| TP31 | DMDSPARE3 | TP32 | GROUND |
| TP33 | VCC_1P8V | TP34 | VCC_1P8V |
| TP35 | PSUHBNT_RST # | TP36 | DMDSPARE0 |
| TP37 | MBRST1_0 | TP38 | 1.0V TEST |
| TP39 | DMDSPARE1 | TP40 | 12V TEST |
| TP41 | VCC_1P0V | | |

# 8 Documentation

This section lists related documents associated with the use of the DDC4000 Controller Board.

2509484 - DLP® Discovery™ 4000 ESD

2509485 - DLP® Discovery™ 4000 Printed Circuit Board (PCB)

2509486 - DLP® Discovery™ 4000 Circuit Card Assembly

2509487 - DLP® Discovery™ 4000 PCB Mechanical Outline Drawing

2509506 - DLP® Discovery™ .95” 1080p interface board ESD

2509507 - DLP® Discovery™ .95” 1080p interface Printed Circuit Board (PCB)

2509508 - DLP® Discovery™ .95” 1080p interface board Circuit Card Assembly

2509509 - DLP® Discovery™ .95” 1080p interface board Mechanical Outline Drawing

2509510 - DLP® Discovery™ 4000 Technical Reference Manual

2509511 - DLP® Discovery™ 4000 Data Sheet

2509512 - DDC4000 Datasheet (DLP® Discovery™ Controller)

www.xilinx.com APPSFPGA development tools and information

www.em.avnet.com/exp EXP specification and products

www.latticesemi.com ECP2 FPGA (DDC4000) information